IEEE
ELECTRON DEVICES SOCIETY
Newsletter

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2017 IEEE International Electron Devices Meeting

December 2–6, 2017, San Francisco
Paper-Submission deadline is August 2nd

63rd International Electron Devices Meeting

The Electron Devices Society's annual technical conference, the 63rd annual IEEE International Electron Devices Meeting (IEDM), will be held in San Francisco, California, U.S.A., from December 2–6, 2017, at the Hilton San Francisco Union Square Hotel.

The IEDM is the world's premier forum for technologists to unveil the best and latest research into electronic, microelectronic, and nano-electronic devices and processes. No other meeting presents as much leading work in so many different areas of microelectronics, encompassing both silicon and non-silicon device and process technology, molecular electronics, nanotechnology, optoelectronics and MEMS (microelectromechanical system) technology.

Highlights of the upcoming IEDM include:

- four plenary presentations by prominent experts
- special focus sessions covering topics in neuromorphics, 3D integration, silicon photonics and bio-nanosensors
- two evening panel discussions
- the IEDM luncheon talk by a prominent industry figure on December 5th
- the Entrepreneur's Lunch at IEDM on December 6th
- tutorial sessions on Saturday afternoon, December 2nd
- two Short Courses on Sunday, December 3rd

Paper-Submission Deadline

The paper-submission deadline is August 2nd for submission of four-page, camera-ready papers. Accepted papers will be published

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Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at edsnewsletter@ieee.org

ELECTRON DEVICES SOCIETY

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EDS Board of Governors (B0G)
Elected Members-at-Large

Elected for a three-year term (maximum two terms) with 'full' voting privileges

2017	Term	2018	Term	2019	Term
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NEWSLETTER EDITORIAL STAFF

Contributions Welcome

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either Editor-in Chief or the Regional Editor for your region. The e-mail addresses of all Regional Editors are listed on this page. E-mail is the preferred form of submission.

Newsletter Deadlines

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at http://eds.ieee.org/eds-newsletters.html. The archive contains issues from July 1994 to the present.

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Upcoming Technical Meetings

2017 IEEE International Integrated Reliability Workshop (IIRW)

The 2017 IEEE International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, will be held at the Stanford Sierra Conference Center on the shores of Fallen Leaf Lake near South Lake Tahoe, California, October 8–12, 2017. This workshop provides a unique forum for open, lively discussions of all areas of reliability research and technology for present and future semiconductor applications.

Reliability topics for the workshop include: SiGe and strained Si, III–V, SOI, high-k and nitrided SiO_2 gate dielectrics, reliability assessment of novel devices, power devices reliability (SiC, GaN), organic electronics, emerging memory technologies (RRAM etc.), NEMS/MEMS, photovoltaics, transistor reliability including hot carriers and NBTI/PBTI, Cu interconnects and low-k dielectrics, product reliability and burn-in strategy, impact of transistor degradation on circuit reliability, reliability modeling and simulation, optoelectronics, single event upsets, array testing as well as the traditional topics of wafer level reliability (WLR) and building-in reliability (BIR). Special topics this year will be on Ferroelectric memory and transistor reliability, FinFET Front End and Back End Reliability, and III–V reliability. For students and early career professionals, there are tutorials on the topics of transistor reliability, chip-to-package interaction and atomistic calculations of device reliability.

The Call for Papers can be found at www.iirw.org. The submission deadline is July 10, 2017. Contact the Technical Program Chair, Luca Larcher (iirw2017@gmail.com) for any further questions or visit www.iirw.org for continued updates about the conference.

IIRW is quite different from a typical technical conference. Located 6400 feet above sea level in the California Sierra Nevada, the Stanford Sierra Conference Center provides an ideal atmosphere for a relaxing yet informative workshop. All aspects of the workshop, including the secluded location, absence of distractions such as in-room phone/television, and the format of the technical program, encourages extensive interaction among the workshop attendees.

Attendees lodge in cabins nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. All rooms have decks with views of Fallen Leaf Lake and the surrounding Sierra peaks. Comfortable and informal dress is encouraged, and meals are provided family-style in the lodge dining room. This peaceful setting presents a terrific opportunity to get to know your colleagues, including internationally renowned experts.

The conference traditionally begins Sunday evening after the majority of attendees arrive. The single Sunday night talk includes refreshments, and is designed for the weary traveler, being a technically toned-down presentation on an interesting topic either peripherally related to reliability, or simply an interesting hobby or business from one of the attendees.

One other advantage of IIRW is the moderated discussion groups that are held in the evenings. Following up on the discussion groups are the Special Interest Groups, which are composed of small groups of attendees who want to continue their discussions on a particular topic of interest, which often continue even after the workshop. Another unique aspect of the workshop is the opportunity for any attendee to present a walk-in poster of their latest work.

Finally, attendees have Wednesday afternoon off to enjoy a variety of outdoor activities such as hiking, volleyball, sailing or kayaking, biking, walking, or simply continuing that intriguing conversation from the night before. This free afternoon is a great way to not only network, but also to build long-lasting friendships.

Additional information about the workshop is available on the IIRW website at www.iirw.org, or by contacting Thomas Kopley, 2017 IIRW General Chair, (gc.iirw@gmail.com). You can also subscribe to our LinkedIn page (https://www.linkedin.com/groups/8245119) for regular updates. Information on the Stanford Camp is available at stanfordsierra.org. Please note, if you want to take part in this event, please register early as space at the Stanford Sierra Conference Center is limited to roughly 120 attendees and the workshop has sold out in the past.

On behalf of the 2017 IIRW Management Committee, I look forward to welcoming you in Lake Tahoe!

Suresh Uppal
2017 IIRW Communications Chair
GLOBALFOUNDRIES, Inc.
Malta, NY, USA

2017 IEEE BIPOLAR/BiCMOS Circuits and Technology Meeting

Miami Marriott Biscayne Bay, Miami, Florida, USA, www.ieee-bctm.org
Conference: October 19–20, 2017; Short Course: October 21, 2017

Foster Dai
General Chair
University of Auburn

Peter Magnée
Technical Program Chair
NXP

On behalf of the IEEE BCTM'17 Executive Committee, we are honored and delighted to invite you to the 2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) at the beautiful Miami Marriott Biscayne Bay, Miami, FL from Oct. 19–21. We invite you to participate at the 2017 BCTM where the highlights include:

- Day-long short-course on **Bipolar transistor device physics and circuit design primer**
  - Prof. John Long, U. Waterloo, Ontario, Canada: Circuit Design
  - Prof. Michael Schröter, TU Dresden, Germany: Device Physics
- Invited papers exploring advances in analog/mixed-signal design, device physics, modeling and simulation, process technology, and wireless design
- Technical papers covering the latest advances in physics, design, performance, fabrication, characterization, modeling, and application of Si/SiGe/SiC bipolar, BiCMOS, and GaN ICs
- Evening dinner banquet

This year the BCTM is co-located with the IEEE Compound Semiconductor IC Symposium (CSICS), which is held at the same location from Oct 22–25.

The IEEE BCTM is a forum for technical communication focused on the needs and interests of the bipolar and BiCMOS community. Papers covering the design, modeling, performance, fabrication, testing and application of bipolar and BiCMOS integrated circuits and devices as well as high-performance circuits using other competitive technologies such as CMOS, SiC, GaN, GaAs, and InP are solicited. Best Paper Awards will be given to the top regular and student papers. A Special Section of the IEEE Journal of Solid-State Circuits will include selected papers from BCTM 2017.

General Contact Information

Visit the conference website: www.ieee-bctm.org or contact: Catherine Shaw, Conference Manager, Phone 1-732-501-3334, e-mail: cshaw.cmpevents@gmail.com

The IEEE BCTM is the world's premier forum focused on the needs and interests of the bipolar and BiCMOS community. If you are interested in leading edge bipolar/BiCMOS devices and technology, circuits, and applications, as well as networking with experts in these areas, please kindly join us this year at the beautiful Miami Marriott Biscayne Bay, Miami, Florida, USA!

47th European Solid State Device Research Conference (ESSDERC)

September 11–14, 2017
Leuven, Belgium

The European Solid State Device Research Conference (ESSDERC) is organized in parallel with the European Solid State Circuits Conference (ESSCIRC). The conference provides an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The increasing level of integration for system-on-chip design made available by advances in semiconductor technology, calls for a deeper interaction among technologists, device experts, IC designers and system designers. While keeping separate Technical Program Committees, the conferences are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

The topics of the 2017 ESSDERC conference are:

- *Advanced CMOS: Process and Device Technology, Characterization and Reliability*
- Opto-, Power and Microwave Devices

- Fundamental Physical Modeling of Materials and Devices
- Device and Circuit modeling
- Advanced and Emerging Memories
- MEMS, NEMS, Bio-sensors and Display Technologies
- Emerging non-CMOS Devices and Technologies

The 2017 edition of the conference includes

- Plenary presentations
  - Françoise Chombar, CEO Melexis, Belgium
    "Engineering a safe, clean and comfortable future"
  - Peter Real, Senior VP & CTO Analog Devices Inc.
    "*Navigating without a Moore's Law Compass"*
  - Hans Stork, Senior VP & CTO ON Semiconductor, USA
    "Smart Power for Automotives"
  - Tetsuo Endo, Professor Tohoku University, Japan
    "Spintronics"
- ESSDERC keynote presentations
  - Ian Young, Intel, Senior Fellow, USA
    "Beyond CMOS Technologies"
  - Siva Sivaram, SanDisk Corp., Executive VP, USA
    "Storage Class Devices"
  - David DiVincenzo, Professor RWTH, Aachen, Germany
    "Control Systems for Quantum Computing"
- ESSCIRC keynote presentations
  - Geert De Peuter, Nokia Bell labs, Belgium
    "The world goes wireless, long-live copper & optical wireline innovations"
  - Sven Mattisson, Ericsson, Sweden
    "Overview of 5G requirements and future wireless networks"
  - Harish Krishnaswamy, Columbia University, USA
    "Integrated Antenna-Interface Components – A Blessing for Wireless Transceivers"
- Invited papers with overall coverage of all aspects of advanced devices and circuits
- Special focused sessions on smart sensors, neuromorphic computing and Beyond CMOS
- Presentation of IEEE and ESSDERC/ESSCIRC Awards
- Conference Gala Diner
- Tutorials
  - Neuromorphic computing with emerging synaptic devices
  - Beyond-CMOS
  - Sensors for the IoT era
  - Integrated power management in research and industry
  - The hidden challenges of 5G'
- Workshops

The conference is organized in Leuven, Belgium. It is the home of the largest university in Belgium, with more than 40000 students. Founded in 1425 by Papal Bull under Martinus V, it is also the oldest university in Belgium. The town and university have known many periods of prosperity. The town hall, churches, cloisters and colleges stand silent witness of those days and make Leuven an interesting place, rich in historical building including the 550 year old town hall, the Great Beguinage, the University Library, the St. Peter's Cathedral and the Papal college. Triggered by the presence of imec, the largest independent research center in Europe with over 3500 researchers coming from more than 75 different countries, Leuven became a world-leading center for micro- and nano-electronics. Leuven is also hosting the headquarters of AB Inbev, the largest brewery in the world.

ESSDERC is financially sponsored by the IEEE Electron Devices Society. For registration and other information, visit the home page at www.essderc-esscirc2017.org or contact Sistema Congressi at essxxrc@sistemacongressi.com

Cor Claeys
Chair Local Scientific Committee
imec/KU Leuven

2017 IEEE International Electron Devices Meeting

(continued from page 1)

as-is, in the proceedings. A limited number of late-news papers, announcing recent developments will be accepted. The deadline for receipt of late-news papers is September 11, 2017. Authors of accepted papers will be notified by the end of September.

Only electronic submissions will be accepted, comprising up to two pages of text and an additional two papers of figures and drawings that describe the planned 20-minute paper presentation and emphasize the findings.

No publication of the submitted work is acceptable prior to the conference.

Topics of Interest

Papers in the following areas are encouraged:

- Circuit and Device Interaction (CDI)
- Characterization, Reliability and Yield (CRY)
- Compound Semiconductor and High Speed Devices (CHS)
- Memory Technology (MT)
- Modeling and Simulation (MS)
- Nano Device Technology (NDT)
- Optoelectronics, Displays, and Imagers (ODI)
- Power Devices (PD)
- Process and Manufacturing Technology (PMT)
- Sensors, MEMS and BioMEMS (SMB)

For more information, visit the IEDM website: www.ieee-iedm.org

Find the IEDM on social media: http://ieee-iedm.org/press/social-media/.

2017 IEDM Committee

Society News

Message from EDS President

Dear EDS Members:

Samar K. Saha
EDS President
(2016–2017)

In continuation to my earlier messages reporting the state of operations of the Electron Devices Society (EDS), I am happy to report that we had a great and productive mid-year Board-of-Governor's (BoG) meeting series during May 20–21, 2017 at Kochi, India. I sincerely thank MK Radhakrishnan, the Vice President of EDS Regions and Chapters, for hosting the meetings in collaboration with EDS Bangalore chapter with meticulous arrangements of events and exquisite foods.

During the meetings, the EDS Executive committee (ExCom) members presented the highlights of the major accomplishments made in the first half of the year 2017. In order to achieve EDS's mission, i.e., sharing technical information among electron devices (ED) community through publications and conferences, professional growth of EDS members through stellar education programs, and recognition of EDS members for their technical achievements and leadership, I am happy to report the major progresses made in these areas in the first half of 2017.

- ***Membership Growth:*** Through our membership drive to grow and retain EDS membership, I am happy to report that through April 2017 our membership grew by 3.5% compared to April 2016 whereas, IEEE membership declined by 2.4% during the same period. EDS also participated in an IEEE multi-society membership drive at the *March for Science* event on April 22, 2017 in Washington, D.C.
- ***Publications Excellence:*** Our open access (OA) publication, the *IEEE Journal of the Electron Devices Society* (J-EDS) is gradually establishing itself as the most preferred OA publication for the ED community with a newly published impact factor (IF) of 3.14. The IF is on the rise for all our world-class flagship publications, the *IEEE Transactions on Electron Devices* (T-ED) and *IEEE Electron Device Letters* (EDL) reaching numbers 2.61 and 3.05, respectively. In addition, the EDL submission to online posting is the best in IEEE, averaging 3.0 weeks. Our publications continue to excel through the self-less dedication and relentless efforts of the Editor-in-Chiefs and their editorial boards.
- ***Conference Management***: We are increasing our conference portfolio to strategically position EDS in the emerging technical areas and strategic geographical locations. The first *IEEE Electron Devices Technology and Manufacturing* (EDTM) conference, held in Toyama, Japan, on February 28–March 2, 2017, was a huge success. The 2018 EDTM is on schedule to be held during March 13–16, 2018 in Kobe, Japan. In order to dive into the newly revitalized flexible electronics technical area, we have also initiated a new conference, *IEEE International Flexible Electronics Technology Conference* (IFETC), in collaboration with IEEE Council on RFID. The first IFETC is scheduled for August 7–9, 2018, in Ottawa, Ontario, Canada. Also, to increase the visibility and attendance of our flagship conferences, we have offered options to the newly elected EDS fellows to be recognized at a conference of their own choice. And, for the first time, we have recognized EDS Fellows at the opening sessions of 2017 *VLSI Technology Symposium* in Kyoto, Japan and the 2017 *Photovoltaic Specialists Conference* (PVSC-44) in Washington, D.C.
- ***Chapter Growth:*** We have modest growth of EDS chapters, reaching a total of 204 through May 2017. Our primary focus is the growth of student chapters to engage students in device research and EDS activities.
- ***Educational Program:*** We are continuing our stellar educational programs including Masters Student and PhD Student Fellowships, Distinguished Lectures (DLs), Mini-Colloquia (MQ), EDS-ETC, Webinars, and so on. Through May 2017, EDS organized three Webinars in emerging technical areas. In addition, we have planned an *Online International College Competition* and an *EDS Center of Excellence* for undergraduate device study to engaging students in EDS.
- ***Outreach Program***: Through our bi-lateral collaboration of mutually beneficial programs with different IEEE Organizational Units (OUs) of common interest, we have several multi-society projects including *Internet of Things* (IoT), *International Roadmaps for Devices & Systems* (IRDS), *Heterogeneous Integration Roadmap* (HIR), and *IEEE 5G* initiatives.

In continuing our effort to outreach programs to students and young professionals, EDS hosted a student social event at the 2017 VLSI Technology and Circuit Symposia on

June 6, 2017, in Kyoto, Japan and a student and Young Professional mixer social event at PVSC-44 on June 25, 2017 in Washington D.C.

- ***Future Directions***: In continuing EDS's usual operations, we have maximized our effort on long-term strategy planning. As we know, the impact of electronic devices from the component to system level on our society is more than ever. This is, especially, true for emerging applications such as automotive, industrial automation, life sciences, security, logistics, mobility, energy saving, social networking, and environmental protection where high growth rates are evident. In particular, device technologies play a key role in nearly all areas of computers, communications, and social media. As the semiconductor industry continues to evolve in providing *smart-electronic devices* enabling solutions for *smart-cars*, *smart-homes*, *smart-city infrastructure*, *Internet of Things and Everything*, and so on, the future of our technical *field-of-interest* (FOI) and therefore, the *broad spectrum and the territory of our Society* will continue to evolve. Thus, it is crucial to have a long-term plan for our society.

In the above context, we had a very successful first EDS strategy planning session on May 20, 2017, in Kochi, India. At this meeting, we discussed self-evaluating the present state of our society, setting long-term goals as the electronic industry evolves, and creating a working document for EDS's first 5-year strategy plan by December 2017. In continuing our discussions at EDS ExCom, we decided to get insights from our membership on self-assessment of our society at present, defining goals for the future, and efficient execution to achieve our long-term goals. So, knowing that EDS members have many of the insights for future, we would like to get your opinion on what the strategic elements for EDS should be in the coming decade. I would appreciate 100% participation from all of you by responding to the questionnaire with your vision for EDS in the long-term.

In summary, the EDS is in good standing with our present goals for the near-future directions and engagements. With your self-less dedication and help, we will create our first 5-year strategic plan building EDS to meet the challenges of the future.

Samar K. Saha
EDS President
Prospicient Devices, CA, USA
samar@ieee.org

Message from Editor-in-Chief

Dear EDS Members and Readers,

Carmen M. Lilley
Editor-in-Chief
EDS Newsletter

As I begin my term as the new Editor-in-Chief (EiC) for the EDS Newsletter, I want to offer my sincerest thank you to M.K. Radhakrishnan for sharing with me his expertise on leading the newsletter and offering constructive feedback on my ideas to further enhance the newsletter to meet member and reader interests and needs. He has been very supportive and always provided detailed answers to editorial questions, while we transitioned to my taking on the full EiC responsibilities for this newsletter. I want to also thank Joyce Lombardini, from the EDS office, for her support, enthusiasm in implementing new ideas, and helping plan future enhancements of the newsletter. Finally, I want to also thank Simon Deleonibus, Chair of the Newsletter Committee, for his insights on implementing changes to the newsletter over the course of the next year.

I am very excited to take on the immense responsibility of the EDS Newsletter and continue enhancing the newsletter, as M.K. successfully did when he became the EiC. I also look forward to working with the Regional Editors to share with you the various activities, news, and highlights of EDS members around the globe. In addition, I hope to streamline the sharing of information, expand the themes that appear in the newsletter, such as professional development articles, and incorporate further improvements that result in a high interest newsletter for our EDS members and readers. I invite our EDS members and readers to share with me their ideas on themes they would like to appear in the newsletter and feedback on changes you see in the newsletter in the coming year.

Sincerely,

Carmen M. Lilley
University of Illinois at Chicago
Editor-in Chief, EDS Newsletter
e-mail: clilley@uic.edu

Highlights of the EDS Board of Governors Forum Meetings

Simon Deleonibus
EDS Secretary

The 2017 mid-year EDS Board of Governors Forum meetings were held in Kochi, Kerala, India, May 20 and 21, 2017. The Crowne Plaza Hotel at Ernakulam, in Kochi metropolitan, was chosen by the local chapters to host the edition of our meeting series. The hospitality and general organization was extremely appreciated; through the meeting arrangements and social events during which Kerala's Mohiniyattam, Kathakali dances and Kalaripayattu martial demonstrations were performed. The whole Forum is indebted to M. K. Radhakrishnan's tireless efforts for the wonderful organization of the meetings and events.

Mid-year updates by the publications and newsletter, education, membership and regions & chapters, and conferences and technical activities Standing Committees were given on Saturday, May 20th and reported by the chairs on Sunday May 21st at the Forum meeting. The ExCom held its meeting as well on Saturday evening. Significant highlights are given hereafter.

The BoG membership reached a quorum at the meeting. That was unfortunately not the case for the Forum. Consequently, the Forum was invited to vote by e-mail on 12 administrative motions, initially planned to be voted at the meeting. The list of these approved motions is given at the end of this article.

Last March 6, 2017, the BoG approved by email vote the revision of 4 Bylaws Sections and 2 Constitutions articles as well as the creation of a new Bylaws section, which were proposed by the Constitution and Bylaws AdHoc Committee, following their presentation and discussion at the December 2016 meeting.

Highlights

Motions approved at the May 21, 2017, BoG meeting requesting future changes to the Constitution and the Bylaws.

Two motions were submitted to the BoG vote by Fernando Guarin, after discussions at the ExCom meetings in February and May 2017 and at the Kochi BoG meeting.

1) *Motion*: To approve the termination of EDS pilot-election of one BoG member-at-large per year by vote of the general membership. Motion passed.
   This pilot program was initiated in 2014 to terminate in 2018 (approved in December 2013, Bylaws section 5.6) and has been unsuccessful in terms of regional representation. Only Regions 1–6 have members at large elected from the general membership. Still we need to address the question of the lack of success of this initiative among the membership of the other regions.
2) *Motion*: To approve for all EDS elected and appointed positions, a given individual shall not serve more than two terms in a given position. *Motion passed*.
   This change is motivated by the necessity to renew the BoG and Forum members and give equal chance to all members to access to the various committees (standing or technical), Forum or BoG. All Committees Charters will need to be revised as well.

Newsletter. The assignment of Carmen Lilley, as new EiC of the EDS Newsletter, was done according to IEEE and EDS policies. Initiatives have been taken to reduce the manufacturing costs and introduce colored graphics. The project emphasizes additional content in a web based newsletter while keeping a streamlined paper version. Editorial changes include: 1) Increasing Technical and Professional contents, including the Young professionals and Women in Engineering sections; 2) To support

Attendees of the 2017 EDS BoG Meeting Forum in Kochi, Kerala, India

Administrative motions voted by the Forum by email in May (deadline May 26, 2017):

Motion: 2017 appointments
Motion: December 2016 EDS meeting minutes
Motion: 2018 mid-year BoG meeting location/dates
Motion: 2018 publication page prices for EDL and T-ED
Motion: 2018 membership dues price of $18
Motion: 2018 publication page budget
Motion: EDS technical co-sponsorship for the 2018 Flexible Electronics Technology Conference and Technical Committee motions
Motion: EDS technical co-sponsorship for the 2017 Fifth Berkeley Symposium
Motion: EDS 100% financial sponsorship for the 2018 Electron Devices Technology and Manufacturing Conference (EDTM)
Motion: Name change of the Organic Electronic Technical Committee to Flexible Electronics and Displays
Motion: Name change of the Vacuum Devices Technical Committee to Vacuum Electronics
Motion: Approve 50% EDS Financial Sponsorship for the Int. Conference on Emerging Electronics (ICEE)
All motions passed.

such a development new positions of Associate Editors by theme, complementing the Regional Editors, would be necessary; 3) Regional news would be posted on the website; 4) Different derivative products (flipbook, email blast, eNewsletter) could be generated from the initial PDF format. A finalized project will be submitted to the BoG/Forum for approval in December 2017, before its implementation in 2018.

Publications. Hisayo Momose reminded us that the publication's cover is the first impression given to the readers of our Journals. EDL EiCT-J King-Liu presented new cover designs utilizing 4-color graphics and incorporating cover lines from editors' picks from current published papers. There was a general consensus to encourage such initiatives to rejuvenate the graphic character of our journals and other communications outreach efforts. Five Special Issues are already defined for the 2017–2018 period. The PPC is invited to suggest subjects one year in advance. The renewal of EiCs in our co-sponsored journals such as JPV and TSM is a timely issue that our EiCs search procedure requests to include.

Conferences and Technical Committees. Our 57 sponsored/co-sponsored conferences are financially safe with some critical points to watch after. The inaugural EDTM Conference, held in Toyama (Japan), had 292 attendees. The 2018 Conference will be held in Kobe, Japan before expanding to other countries in Asia. In the discussion, Technical Committees, Conferences Committees and our PPC were encouraged to work together and be proactive to suggest Special Issues in our Journals.

Regions and Chapters. To enforce the credibility of our chapters and their sustainability, a minimum chapter presence has been determined to be 12 members. The number of chapters has increased substantially in 2016 (204 by May 2017). The situation might be critical in terms of chapters strength especially for the students chapters and has to be analyzed region by region. M. K. Radhakrishnan reminded us that a chapter subsidy is linked to their reporting, which needs to be improved. As well, the DL and MQ programs will undergo revamping in order to maintain top quality: 1) apply strictly the rule of 2 lectures minimum given in 2 years to keep the DL title; 2) a yearly budget per Lecturer is defined ($2,500 per Lecturer per year); 3) limit the number of Distinguished Lecturers to 1% of EDS members; 4) define regional EDS tutorials; and 5) propose an "Eminent Lecturers" Program.

Education. Mansun Chan updated the group on the different initiatives of EDS' Education programs. Webinars are very popular thanks to the choice of timely relevant subjects. The Electronic Exploration Camps initiatives (middle school level) are being repeated thanks to their success already obtained in Regions 9 and 10. This initiative is projected to expand to other locations in 2017. A strong interaction with the R. & C. Committee will be essential to the success of this policy.

Membership. Tian-Ling Ren launched the Membership presentation with some good news: EDS Membership in February reached a recent high. Despite the deactivation of arrears (removal of non-renewing members) the following month, EDS' membership in April 2017 was 3.5% greater than April 2016 and sharply up compared with the decrease in IEEE membership during the same period (–2.4%). We are pursuing our membership development growth by proceeding with several measures: 1) monthly e-mail reminders to members and promotional campaigns; 2) agreements with other IEEE societies; 3) onsite enrollments at conferences; 4) IEEE sponsored YP events; 4) promotions at MQs and DLs; 5) outreach to EDS members eligible to become Senior, etc.

5-Year plan for EDS. All Standing and Technical Committees members as

well as the general membership will be requested to contribute to the white paper on the EDS 5 year plan in May 2018. The document will be presented at the BoG/Forum meeting in December 2017.

Inputs on the Strategic Plan from each committee were due at EDS HQ Office by July 15th. Reports are due to the Executive Office by August 15th. Jim Skowrenski will review the reports and work on a first draft due in October.

Simon Deleonibus
EDS Secretary

Report of EDS Region 10 Meeting

EDS BoG Meeting, Kochi, India—May 2017

The EDS Region 10 Meeting was held during the BoG/Forum meetings series in Kerala on the afternoon of May 20, 2017. The meeting gathered 30+ attendees from all regions and mainly Region 10 Chapters Chairs and Representatives (13). For the meeting preparation, all Region 10 Chapter Chairs were requested by the Region 10 SRC Chair, Ru Huang, to send reports of their chapter's recent activities. After introductory remarks and data presentations by both M. K. Radhakrishnan, EDS Vice President of Regions and Chapters and Ru Huang, the Chapters Chairs and Representatives were invited to comment and following points were discussed:

From L-R – SRC Vice Chairs (Dr. Manoj Saxena, Dr. Anisul Haque), Dr. M. K. Radhakrishnan (EDS VP RC Committee), Dr. Samar Saha (EDS President), Dr. Fernando Guarin (EDS President Elect), Dr. Ru Huang (SRC Chair Region 10), Dr. Soumya Pandit (RC member), Prof. Navakant Bhat (BoG member) and Dr. Mayank Srivastava (Chapter Chair, EDS/SSC Bangalore, India)

- Region 10 is the widest region for IEEE and includes 2,885 members, 68 chapters, among which 21 are 100% EDS, 17 are Joint Chapters and 30 Students Chapters. It has the largest proportion of 100% EDS and Student Chapters among all regions.
- The formal reporting of our Chapters to the IEEE EDS headquarters was analyzed and commented, through the use of common metrics. The available data included L31 forms, MQ and DL deliveries, and EDS Newsletter reporting. In 2016, the Malaysia Chapter organized a maximum of 37 activities followed by the Delhi Chapter with 20. Amongst the student branch chapters, ED Sri Jayachamarajendra College of Engineering Student Branch Chapter, India, organized the most activities (17) in Region 10. Region 10 has 15 chapters which have organized less than 4 technical activities. There are at least 6 dormant/weak Student Chapters which have student members less than the minimum, and 1 student chapter has been recommended for closure. For the rest of the weak chapters, the RC and SRC team members are now actively engaging in reviving them.
- The possible reasons for inactive chapters were discussed and based on the geographic location of the inactive chapters, it was decided that R10 members along with RC/SRC members take charge of different sub-regions and shall visit at least one inactive chapter in 2017. Region 10 members can suggest chapter adjustment if needed, such as chapter merging or chapter cooperating with another society.
- A detailed discussion was carried out on new chapter formations. It was presented that the chapter student member strength has remained nearly the same in the past 10 years. However, the number of chapters has increased significantly and in many chapters, student membership has gone below the required level. Therefore, it was recommended that the minimum student membership for student chapters should be 12; RC team members should periodically review chapter performance; strong device research must be one of the criteria for chapter formation; and all non-revivable chapters should be closed.

Ru Huang
Region 10 SRC Chair

Manoj Saxena
Region 10 SRC Vice Chair

Call for Nominations—EDS Board of Governors

Albert Wang
Chair of EDS Nominations & Elections

The IEEE Electron Devices Society invites nominations for election to its Board of Governors—BoG (formerly AdCom) members-at-large. The next election will be held after the BoG meeting on Sunday, December 3, 2017. This year, eight out of the twenty-two members will be elected for a 3-year term, with a maximum of two terms.

According to the two related motions passed at the mid-year BoG meeting held in Kochi, India, on May 21st, a member can only serve for a maximum of two terms as a BoG member in a life time and the pilot program for one of the BoG Member-at-Large seats to be elected via the entire EDS membership will be discontinued going forward. Therefore, the eligibility will be verified for all nominees who will be voted on by the EDS BoG. All electees begin their term in office on January 1, 2018. The nominees need not be present to run for the election. In 2017, eight positions will be filled.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor and Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Constitution and Bylaws. The electees are expected to attend both BoG Meetings every year. While the December meeting is organized in connection with the IEEE International Electron Devices Meeting, the mid-year meeting is frequently held outside the US. Partial travel support is available to attend both of these meetings.

All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. It is the responsibility of the nominators and the endorsers to make sure that, if elected, the nominee is willing to actively serve in the position as a BoG member-at-large.

Please submit your EDS BoG nomination by October 15, 2017, using the online nomination form (https://ieeeforms.wufoo.com/forms/k4vnyad0ys3o4z/).

Also, all endorsements letters should be sent to the EDS Executive Office, Laura J. Riello via e-mail: l.riello@ieee.org by October 15, 2017. If you have any questions, please feel free to contact Laura Riello (l.riello@ieee.org) with a copy to me at aw@ece.ucr.edu.

Albert Wang
Chair of EDS Nominations & Elections
University of California
Riverside, CA, USA

EDS Board of Governors (BoG) Members-at-Large Election Process

The Members-at-Large (MAL) of the EDS Board of Governors are elected for staggered 3-year terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from each of the following geographic areas: Regions 1–7 and 9; Region 8; and Region 10. In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected BoG member is a Young Professional (YP—formerly Gold member). A Young Professional member is defined by IEEE as a member who graduated with his/her first professional degree within the last fifteen years. It is also required that there are at least 1.5 candidates for each opening. On May 20, 2017, the BoG approved to set a life time limit of two terms for a volunteer to serve as a BoG Member-at-Large, which must be considered for nominations. The EDS BoG also approved to discontinue the pilot program for one of the BoG Member-at-Large seats to be elected via the entire EDS membership. Accordingly, all nominees will be voted on by the EDS BoG in its meeting in December, 2017. All electees begin their term in office on January 1, 2018. The nominees need not be present to run for the election. In 2017, eight positions will be filled.

The election procedure begins with the announcement of Call for Nominations in the *EDS Newsletter*. The slate of nominees is developed by the EDS Nominations & Elections Committee. Nominees are asked to submit a twopage biographical resume and an optional 50 word personal statement in a standard format.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing &

Technical Committee Chair/Member, Publication Editor & Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Bylaws. All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. Self-nomination is allowed. Endorsers should send a brief email to Laura Riello stating that they would like to endorse the candidate. Please note that there is no limit to the number of candidates that a full voting BoG member can endorse.

The deadline for Nominations will be October 15, 2017. The biographical resumes and endorsement letters will be distributed to the BoG prior to the December BoG meeting. The election will be held after the conclusion of the BoG meeting in December 2017.

Albert Wang
Chair EDS of Nominations & Elections
University of California
Riverside, CA, USA

EDS Chapter Subsidies for 2018

The deadline for EDS chapters to request a subsidy for 2018 is September 1, 2017. For 2017, the EDS BoG awarded funding to 75 chapters, with most amounts primarily ranging from US$500 to US$1,000. In June, Chapter Chairs were sent an email notifying them of the current funding cycle and providing them with a list of guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion, travel allowances for invited speakers to chapter events, and support for student activities at local institutions.

Chapter Subsidies can be requested by completing the EDS Chapter Subsidy Request Form http://eds.ieee.org/chapter-subsidy-program.html. Please note that the request needs to be submitted by September 1st.

Final decisions concerning subsidies will be made in December. Subsidy checks will be issued by early January of the following year. Please visit the EDS website http://eds.ieee.org/chapter-subsidy-program.html for more information.

Enhance Your Career with IEEE Senior Membership!

Tian-Ling Ren
EDS Vice-President of Membership and Services

The Electron Devices Society established the EDS Senior Member Program to both complement and enhance the IEEE's Nominate-a-Senior-Member Initiative and make IEEE/EDS members aware of the opportunity and encourage them to elevate their IEEE membership grade to Senior Member. This is the highest IEEE grade for which an individual can apply and is the first step to becoming a Fellow of IEEE. If you have been in professional practice of 10 years, you may be eligible for Senior Membership.

Benefits of Senior Membership[1]

- **Leadership Eligibility:** Senior members are eligible to hold executive IEEE volunteer positions.
- **Recognition:** The professional recognition of your peers for technical and professional excellence.
- **Senior member plaque:** Since January 1999, all newly elevated Senior members have received an engraved Senior Member plaque to be proudly displayed for colleagues, clients and employers to see. The plaque, an attractive fine wood with bronze engraving, is sent within six to eight weeks after elevation.
- **US$25 coupon:** IEEE will recognize all newly elevated Senior members with a coupon worth up to US$25. This coupon can be used to join one new IEEE society. The coupon expires on 31 December of the year in which it is received.
- **Letter of commendation:** A letter of commendation will be sent to your employer on the achievement of Senior member grade (upon the request of the newly elected Senior member).

[1]IEEE.org, http://www.ieee.org/membership_services/membership/senior/index.html

- **Announcements:** Announcement of elevation can be made in section/society and/or local newsletters, newspapers and notices.
- **Ability to refer other candidates:** Senior members can serve as a reference for other applicants for senior membership.
- **Review panel:** Senior members are invited to be on the panel to review senior member applications.
- **US$25 referral coupon:** Newly elevated Senior members are encouraged to find the next innovators of tomorrow and invite them to join IEEE. Invite them to join and the new IEEE member will receive $25 off their first year of membership.

As part of the IEEE's Nominate-a-Senior-Member Initiative, the nominating entity designated on the member's application form will receive US$10 from IEEE for each application approved for Senior Member grade when there are at least five approved applications. As an EDS member, we would appreciate it if you could indicate on your Senior Member application form that **EDS** is your nominating entity.

Please be aware that even if you decide to list EDS as your nominating entity, you still need to have an IEEE member nominate you along with two other references. Your nominator and your references all must be active IEEE members holding Senior Member, Fellow or Honorary Member grade.

For more information on the criteria for elevation to Senior Member, please visit the Senior Membership Portal: http://www.ieee.org/membership_services/membership/senior/index.html.

We strongly encourage you to apply for IEEE Senior Membership to enhance your career. At the same time, you'll be helping EDS. Thank you for supporting IEEE and EDS.

Tian-Ling Ren
EDS Vice-President of
Membership and Services
Tsinghua University
Beijing, China

IEEE Annual Election—Don't Forget to Vote!

This is a reminder for EDS members to vote in the 2017 IEEE Annual Election for the following positions and candidates. Listed below are the positions and candidates that will appear on the 2017 IEEE Annual Election ballot.

Position	Candidate
IEEE President-Elect, 2018	• Jóse M. F. Moura (Nominated by Petition) • Vincenzo Piuri (Nominated by IEEE Board of Directors) • Jacek M. Zurada (Nominated by IEEE Board of Directors)
IEEE Region 1 Delegate-Elect/ Director-Elect, 2018–2019	• Ali Abedi (Nominated by IEEE Region 1) • Eduardo F. Palacio (Nominated by IEEE Region 1)
IEEE Region 3 Delegate-Elect/ Director-Elect, 2018–2019	• Jill I. Gostin (Nominated by IEEE Region 3) • John Kenneth Pigg (Nominated by IEEE Region 3)
IEEE Region 5 Delegate-Elect/ Director-Elect, 2018–2019	• James R. Look (Nominated by IEEE Region 5) • Timothy R. Weil (Nominated by IEEE Region 5)
IEEE Region 7 Delegate-Elect/ Director-Elect, 2018–2019	• Jason Jianjun Gu (Nominated by IEEE Region 7) • Adam Skorek (Nominated by IEEE Region 7)
IEEE Region 9 Delegate-Elect/ Director-Elect, 2018–2019	• Enrique A. Tejera M. (Nominated by IEEE Region 9) • Alberto Sanchez (Nominated by IEEE Region 9)
IEEE Standards Association President-Elect, 2018	• Dennis B. Brophy (Nominated by IEEE Standards Association) • Robert S. Fish (Nominated by IEEE Standards Association)
IEEE Standards Association Board of Governors Member-at-Large, 2018–2019	• Masayuki Ariyoshi (Nominated by IEEE Standards Association) • Walter Weigel (Nominated by IEEE Standards Association)
IEEE Standards Association Board of Governors Member-at-Large, 2018–2019	• Stephen D. Dukes (Nominated by IEEE Standards Association) • Robby Robson (Nominated by IEEE Standards Association)
IEEE Technical Activities Vice President-Elect, 2018	• K.J. Ray Liu (Nominated by IEEE Technical Activities) • Douglas N. Zuckerman (Nominated by IEEE Technical Activities)
IEEE-USA President-Elect, 2018	• Thomas M. Coughlin (Nominated by IEEE-USA) • Guruprasad "Guru" Madhavan (Nominated by IEEE-USA)

Balloting period starts on 15 August and ends at 12:00 noon, Central Time USA (17:00 UTC) on 2 October 2017. All eligible voting members should look for their ballot package to arrive via postal mail or access it electronically at www.ieee.org/elections. For more information on the election and candidates, visit the IEEE Annual Election Web page at www.ieee.org/elections, or email election@ieee.org.

2017 IEEE William R. Cherry Award Winner

Prof. Eli Yablonovitch, Director of the NSF Center for Energy Efficient Electronics Science headquartered at Berkeley, received the William Cherry Award in recognition of his many contributions to solar cell device physics and technology.

Although Yablonovitch has worked in a variety of pure and applied fields, his first love has always been Photovoltaics, which he regards as part of the same double-heterostructure family as LED's and semiconductor lasers. In his photovoltaic research, he introduced the 4(n squared) ("Yablonovitch Limit") light-trapping factor that is in worldwide use for almost all commercial solar panels. He also published research on the fundamental efficiency limits in solar cells and developed novel surface passivations for silicon and GaAs.

His mantra that "a great solar cell also needs to be a great LED," is the basis of the world record solar cells: single-junction 28.8% efficiency; dual-junction 31.5% at Alta Devices Inc.; & quadruple-junction 38.8% efficiency in NREL; all at 1 sun.

Eli Yablonovitch introduced the idea that strained semiconductor lasers could have superior performance due to reduced valence band (hole) effective mass. With almost every human interaction with the internet, optical telecommunication occurs by strained semiconductor lasers.

Eli Yablonovitch

He is regarded as a Father of the Photonic BandGap concept, and he coined the term "Photonic Crystal". The geometrical structure of the first experimentally realized Photonic band gap, is sometimes called "Yablonovite."

Eli has founded or cofounded several companies, including Ethertronics, Inc., (cellphone antennas) and Luxtera (originator of Silicon Photonics).

Prof. Yablonovitch is elected as a Member of the National Academy of Engineering, the National Academy of Sciences, the American Academy of Arts & Sciences, a Foreign Member of the Royal Society of London, and has received numerous other prestigious awards.

He received his Ph.D. degree in Applied Physics from Harvard University in 1972, worked for two years at Bell Telephone Laboratories, and then became a professor of Applied Physics at Harvard. In 1979 he joined Exxon to do research on photovoltaic solar energy. Then in 1984, he joined Bell Communications Research, where he was Director of Solid-State Physics Research. In 1992 he joined the University of California, Los Angeles, prior to joining U. C. Berkeley as Professor of E.E. and Computer Sciences, where he holds the James & Katherine Lau Chair in Engineering.

Ronald A. Sinton
2017 Cherry Award Chair

44th Photovoltaic Specialists Conference (PVSC) Young Professional Award Winner

The IEEE Photovoltaics Specialists Conference (PVSC) continued this year in recognizing an outstanding young professional in the photovoltaics (PV) community. The PVSC Young Professional Award recognizes individuals who have made significant contributions to the science and technology of PV energy conversion, including work on PV materials, devices, modules, and/or systems. The award recipient must also show significant promise as a leader in the field.

On behalf of the organizing and program committees of the 44th IEEE PVSC, I am delighted to announce the recipient of this year's award—**Ms. Weiwei Deng** (State Key Laboratory of PV Science and Technology at Trina Solar). She is recognized for her work as the main contributor responsible for the development of very-high-efficiency Mono and Multi PERC solar cells, which have recently reached several new world records for industrial low-cost silicon solar cells.

Ms. Weiwei Deng received her Bachelor Degree in Materials Science

Engineering in 2005 from Wuhan University of Technology and her Masters Degree in 2007 from the same university. She completed her Master thesis on Study of Dielectric Materials at the State Key Laboratory of Advanced Technology for Material Synthesis and Processing, Wuhan University of Technology.

After her graduation, she started working at Trina Solar as a researcher in the Advanced Solar Cell group, focusing on high-efficiency p-type silicon solar cells. During the past seven years at the State Key Laboratory of PV Science and Technology, she and her team worked exclusively on PERC solar cell research, optimizing the cell design and process for large-volume industrial manufacturing. Five efficiency world records on mono and multi P-type solar cell were achieved by her team. The most recent records are a total-area efficiency of 22.61% for mono PERC solar cells and 21.25% for multi PERC solar cells, all made on standard substrates of 156 × 156 mm with low-cost industrial processes. Several records of module efficiency were also made possible thanks to the cells that she developed.

Weiwei Deng

Ms. Weiwei Deng is currently senior manager of the PERC solar cell research team at the State Key Laboratory of PV Science and Technology at Trina Solar. She is author or co-author of 13 scientific papers and 11 patents related to photovoltaics. Over the last few years, she and her team have managed to continuously improve the efficiency of mono- and multi-crystalline silicon PERC solar cells, pushing the limits of technology and surpassing their previous records. She is dedicated to demonstrate all the possibilities of PERC technology on an industrial scale, and to approach as close as possible to the 25% efficiency level that was achieved by researchers in the laboratories of The University of New South Wales more than 17 years ago.

Congratulations, Ms. Deng!

Geoffrey Bradshaw
Awards Chair, PVSC-44
Air Force Research Laboratory

2017 EDS Chapter of the Year Award Call for Nominations

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st–June 30th period.

Each year EDS will award one Chapter from each of the following Regions:

- Regions 1–7
- Region 8
- Region 9
- Region 10

Nominations for the awards can only be made by SRC Chairs/Vice-Chairs, Regions/Chapters Committee Members or self-nominated by Chapter Chairs. Please visit the EDS website to submit your nomination form (http://eds.ieee.org/chapter-of-the-year-award.html).

Each winning chapter will receive a plaque and check for $500 to be presented at an EDS chapter meeting of their choice. Travel reimbursement will not be provided.

The schedule for the award process is as follows:

Action	Date
Call for nominations e-mailed to chapter chairs, SRC Chairs, SRC Vice-Chairs and Regions/ Chapters Committee	June 1st
Deadline for nominations	September 15th
Regions/Chapters Committee & SRC Chairs & Vice Chairs selects winners	Early October
Award given to chapter representative at requested chapter meeting	Open

EDS Members Recently Elected to IEEE Senior Member Grade

Mohammad Abdul Alim
Srabanti Chowdhury
James Coooper
Nor Hisham Hamid
David Horsley
Francesca Iacopi
Siti Ibrahim*
Babulu K.
Georgios Konstadinidis
Sarah Kurtz
Duu Sheng Ong
Nezih Pala
Toomas Rang
Changhwan Shin
Volker Sorger
Vyshnavi Suntharalingam
Xingsheng Wang
Zubaida Yusoff*
Nor Za'bah
Linton Salmon*

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status. For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html.

To apply for senior member status, fill out the on-line application after signing in with your IEEE account: https://www.ieee.org/membership_services/membership/senior/application/index.html. *Senior Members who remembered to designate EDS as their nominating entity.

Please remember to designate the Electron Devices Society as your nominating entity!

IEEE Journal of the Electron Devices Society

The IEEE Journal of the Electron Devices Society (J-EDS) is a peer-reviewed, open-access, fully electronic scientific journal publishing papers ranging from applied to fundamental research that are scientifically rigorous and relevant to electron devices.

Please submit your manuscripts for consideration of publication in J-EDS at http://mc.manuscriptcentral.com/jeds.

The J-EDS publishes original and significant contributions relating to the theory, modelling, design, performance, and reliability of electron and ion integrated circuit devices and interconnects, involving insulators, metals, organic materials, micro-plasmas, semiconductors, quantum-effect structures, vacuum devices, and emerging materials with applications in bioelectronics, biomedical electronics, computation, communications, displays, micro-electromechanics, imaging, micro-actuators, nano-devices, optoelectronics, photovoltaics, power IC's, and micro-sensors. Tutorial and review papers on these subjects are also published.

As an open-access title, J-EDS provides the electron devices community:

- Faster speed of publication
- Free access to readers globally
- World-wide audience
- Increased dissemination
- High impact factor (IF)
- Articles can be cited sooner
- Articles potentially cited more frequently

ELECTRON DEVICES SOCIETY®

Call for Nominations

2016–2017 IEEE Electron Devices Society
Region 9 Biennial Outstanding Student Paper Award

Description: Awarded to promote, recognize, and support meritorious research achievement on the part of Region 9 (Latin America and the Caribbean) students, and their advisors, through the public recognition of their published work, within the Electron Devices Society's field of interest: All aspects of the physics, engineering, theory and phenomena of electron and ion devices such as elemental and compound semiconductor devices, organic and other emerging materials based devices, quantum effect devices, optical devices, displays and imaging devices, photovoltaics, solid-state sensors and actuators, solid-state power devices, high frequency devices, micromechanics, tubes and other vacuum devices. The society is concerned with research, development, design, and manufacture related to the materials, processing, technology, and applications of such devices, and the scientific, technical and other activities that contribute to the advancement of this field.

Prize: A distinction will be conferred in the form of an Award certificate bestowed upon the most outstanding Student Paper nominated for the two-year period. The prize will be presented at either the International Caribbean Conference on Devices, Circuits and Systems (ICCDCS) or the Symposium on Microelectronics Technology and Devices (SBMicro). In addition to the recognition certificate, the recipient will receive a subsidy of up to $1,500 to attend the conference, where the award is to be presented. There will be a formal announcement of the winner in a future issue of the EDS Newsletter. The winner will also receive up to three years of complimentary IEEE and EDS student membership, as long as winner remains eligible for student membership.

Eligibility: Nominee must be enrolled at a higher education institution located in Region 9. In the case of a co-authored paper, only eligible co-authors may be nominated. Papers should be written in English on an electron devices related topic. Papers should have been published, in full-feature form, during 2016–2017 in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics. Statements by the student and by the faculty advisor should accompany the nomination. Nominator must be an IEEE EDS member. Previous winners of this award are ineligible. There must be a minimum of five nominations submitted in order for the award to be administered for that year.

Basis for Judging: Demonstration of Nominee's significant ability to perform outstanding research and report its results in the field of electron devices. Papers will be judged on: technical content merit, originality, structure, clarity of composition, writing skills, overall presentation. These criteria will be weighted by the assessment of the nominee's personal contribution and the linkage of the nominated work to the nominee's career plans.

Nomination Package:

- Nominating letter by an EDS member (it may be the faculty advisor)
- A brief one-page (maximum) biographical sketch of the student
- 1000 words (maximum) statement by the nominated student describing the significance and repercussion of the nominated work within the wider scope of the nominee's career plans
- A 400 words (maximum) statement by the faculty advisor under whose guidance the nominated work was carried out. It should unmistakably state the faculty advisor's support of the nomination, and clearly explain the extent of the nominated student's contribution, as well as its relevance for the overall success of the reported work.
- A copy of the published paper

Timetable:

- Nomination packages are due at the EDS Executive Office no later than **15 February 2018**.
- Nomination packages can be submitted by mail, fax or e-mail, but a hard copy must be received at the EDS Office
- Winners will be notified by 15 March 2018.
- Recipients may choose to have the formal presentation of the award at either one of the conferences: ICCDCS 2018 or SBMicro 2018

Send completed package to:
IEEE Operations Center
EDS Executive Office
EDS R9 Outstanding Student Paper Award
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:
Laura Riello, EDS Executive Office
l.riello@ieee.org or 732-562-3927

Young Professionals

Reflections from EDS Young Professionals

Vivianne Estefania Niño Vega

The IEEE EDS Newsletter would like to hear from IEEE Young Professionals who as EDS members would like to share their thoughts and experiences with other members.

We hope you enjoy reading about our featured Young Professional in this issue, Vivianne Estefania Niño Vega.

As a young professional, why do you consider the membership in IEEE and especially in EDS important?

I have been a volunteer with IEEE for over 4 years, I began as a student member when I was just starting my bachelor's degree in Electrical Engineering, and it has been a great experience. I have worked directly with EDS in societal outreach through the EDS-ETC Program, allowing me to witness, not only the huge potential that children have for learning about electronic devices, but also, the impact that can be generated in the long-term by sharing this knowledge. Those elements generate the most value for me as a member of IEEE and EDS.

The EDS Tunja Chapter was recently awarded the Region 9 Chapter of the year Award. Can you please tell us about the activities that the chapter has been conducting, especially in terms of engineering social outreach, and your involvement in those activities?

The EDS Student Chapter in the Universidad Santo Tomas de Tunja (USTA) has been following over the years a path of work excellence hand-to-hand with its members, volunteers, and advisors. There has been a collaboration between the chapter and the student branch to develop important regional activities with social outreach throughout the region. In my role as chair of the student chapter from 2014 to 2016, I have participated and lead several of these events. Furthermore I have promoted and organized other events as "Navidad FIEEEliz" and "Maleton."

The "Engineers Demonstrating Science: An Engineer Teacher Connection" (EDS-ETC) Program, is the flagship project of our EDS chapter. It is focused on creating technological impact in the Boyaca region, especially in those areas in which there is little knowledge of the different technological tools provided by Electrical Engineering. Using simple and easy-to-use experiments in the classrooms of the schools of the region, this program has become a teaching-tool for technology, especially for electrical engineering. Moreover, we have reached a large number of children in the schools of Boyaca and results have been extraordinary.

The EDS chapter, sponsored by EDS and the Electrical Engineering Department of the University, has also been able to organize several different academic events, like small congresses, and mini-colloquiums. In those events we have had the opportunity to host several distinguished speakers as in the case of Fernando Guarin, Jacobus Swart, Hiroshi Iwai, Roberto Murphy, Edmundo Gutierrez, Stewart Rausch, and Daniel Camacho. Through their lectures, they have all promoted learning and knowledge transfer in the areas of interest of EDS in our University.

We have also organized two events with an exclusive social outreach focus: "Navidad FIEEEliz" and "Maleton." The first one is a project with the objective of providing a day of pure happiness to children with disabilities, social vulnerabilities, and poverty around Tunja, during Christmas time. We have held this event three times from 2014 to 2016, reaching out to more than 600 children, bringing gifts and educational activities. This activity put in evidence the situation of poverty in the outskirts of the city, which lead to the development of the second social activity "Maleton." The goal was to collect as many new bag packs and basic school kits as possible to provide to the children in our communities, so they can attend school in better conditions.

With all these activities, the EDS chapter in USTA Tunja has tried to focus most of its efforts on education, as a fundamental piece for the development of society.

What was the specific reason, if any, which made you to join the largest professional organization in the globe at first, and to select EDS as your favorite Society?

My motivation can be traced back to several circumstances. First, being part of an organization with the history of IEEE, allows me to explore and learn of engineering in aspects that go well beyond the classroom. Second, the societal outreach activities that I mentioned before are an invitation to understand that engineering is much more than data and machines, but the chance to improve society. With respect to EDS, I'm still learning about its benefits and areas of interest and how they match my professional career aspirations.

As a Young Professional (YP) what are your interests, which coincide with

EDS activities and your own technical field? How does your professional life blend with the services you perform as an EDS member/volunteer?

The constant flow of state-of-the art topics in electron devices, allows me to have a broad perspective over the possibilities of engineering in many fields, that itself is a huge professional benefit. Furthermore, as I'm about to finish my undergraduate studies, it is very important for me to strengthen my knowledge and to define the areas in which I want to develop my career, and EDS has been instrumental in this.

As a YP, how do you consider EDS as a focused professional group? What are the changes or developments you would like to see evolve from EDS as a group devoted to humanity and its causes?

From my point of view, EDS is fulfilling its mission to stimulate the growth of its members, especially the younger ones through the initiatives that are being conducted by the student branches. This generates an active participation of young professionals and students in research and knowledge sharing and exchange. I know EDS is an organization that will continue promoting education and the use of electronic devices for the benefit of humanity.

As an EDS YP and a young researcher in the field, how do you consider the prospects of scientific research in this field for the progress of humanity as a whole? Also, in your opinion what possible ways can young researchers and professionals around the globe contribute to the development of a peaceful, global human society?

I believe that nanotechnology can impact and benefit humanity. It is a field where scientific research would have a positive impact in society, enabling the progress of humanity.

The way to contribute to the development of humane, global and peaceful society is Education. I believe that EDS, as an important part of IEEE, is winning the effort in its educational activities and is a key piece to the future of engineering and its introduction to the next generation.

What are your specific suggestions and recommendations for those young professionals who may aspire to join EDS?

Being part of EDS, brings along very interesting opportunities as its field of interest touches every field in engineering. Furthermore the excellence and knowledge associated to EDS, pushes oneself to excel in everything that involves manufacturing of electron devices.

Biography

Vivianne Estefania Niño Vega*, was born in Tunja, Boyaca, Colombia in 1996. In 2012, she graduated from high school in the Escuela Normal Superior Leonor Alvarez Pinzon in Tunja, with an emphasis in teaching. She is currently in her last year of her undergrad studies in Electrical Engineering in the Universidad Santo Tomas in Tunja, where she received the Talento Digital scholarship. She has been an active member of the IEEE Student chapter in her college. She was president of the EDS chapter from 2014 to 2016, and she also chaired the Women in Engineering affinity group during the same time, and a member of the Sight Colombia committee. She is currently studying in the Universidad de Jaen in Spain as an exchange student.*

Two New Webinars Available in the EDS Collection

Anatomy of a Power MOSFET and Emerging Interconnect Technologies for Nanoelectronics

EDS is many things to its members—scientific publisher, technical conference sponsor, networking resource—but at its core EDS is a community of learning. From undergraduate students and PhD candidates to tenured professors and world-renowned researchers, EDS provides device engineers from across the spectrum engaging and enriching educational opportunities.

As part of our commitment to enhancing the value of membership in EDS, we are pleased to present the EDS Webinar Archive. The online collection provides our members with on-demand access to streaming video of past events. The following recently held webinars can be accessed here: http://eds.ieee.org/webinar-archive.html.

Anatomy of a Power MOSFET

Presented by: Dr. Phil Rutter

Phil Rutter is the Power MOSFET technology architect at Nexperia.

He has worked at Nexperia (formerly NXP Semiconductors & Philips Semiconductors) since 1996 and his career there has involved a wide spectrum of power devices ranging from high voltage DMOS, SOI LDMOS, and GaN HEMTs, to low voltage Schottky diodes and trench MOSFETs. As manager of the Advanced Devices

group he is currently responsible for developing next generation power MOSFETs with primary focus on voltages ≤60 V. His research interests involve optimizing both technology and design to specific applications, which arose from his team's work in bringing the world's first DrMOS product to market in 2004.

Phil gained a MEng in Electronics at Southampton University, UK in 1992 and was awarded an MSc and PhD in Semiconductor Devices at University of Manchester in 1993 and 1995, respectively. He has co-authored many peer-reviewed papers and currently holds 20 granted US patents. He is currently serving on the Low Voltage Technical Committee of the ISPSD and the program committee of the Power Supply on Chip Workshop.

Abstract

Since their introduction in the 1970s, silicon power MOSFETs have become the dominant switching element used for power conversion at mains voltages and lower. The relentless drive towards lower conversion losses, smaller size, and lower cost has resulted in this 'simple' switch becoming a highly optimized and complex component. The high level of innovation in this area has led to the evolution of many competing device structures, each with its own advantages and disadvantages depending on the application in which it is used. Common figures of merit, such as $Q_{GD} \bullet R_{DS(ON)}$ and $Q_G \bullet R_{DS(ON)}$, can no longer be used as a realistic estimation of device performance as packaging, reverse recovery, output capacitance, EMI suppression, ruggedness, reliability etc. can also be critical. The design of the MOSFET also has a major impact; poor design can turn a great technology into a mediocre product. The target application ultimately determines what is considered a high performance product, and this can vary wildly depending on the design goals (e.g. size, cost, efficiency, reliability, and time to market). For example, the requirements for a voltage regulator are not necessarily the same as for hot swap.

This on-line seminar dissects a modern low voltage Power MOSFET, discussing how the many factors involved in making a high performing device interact and conflict with each other, and how they are fundamentally limited.

Emerging Interconnect Technologies for Nanoelectronics

Presented by: Prof. Krishna Saraswat

Krishna Saraswat is the Rickey/Nielsen Chair Professor in the School of Engineering, Professor of Electrical Engineering and by courtesy Professor of Materials Science & Engineering at Stanford University. He also has an honorary appointment of an Adjunct Professor at the BITS, Pilani, India. He received his Ph.D. from Stanford University and B.E. from BITS, Pilani. His research interests are in new and innovative materials, structures, and process technology of silicon, germanium and III–V devices and metal and optical interconnects for nanoelectronics, and high efficiency and low cost solar cells. Prof. Saraswat has supervised more than 85 doctoral students, 30 post-doctoral scholars and has authored or co-authored 15 patents and over 750 technical papers, of which 10 have received *Best Paper Award*. He is a Life Fellow of the IEEE. He received the Thomas Callinan Award from The Electrochemical Society in 2000, the 2004 IEEE Andrew Grove, Inventor Recognition Award from MARCO/FCRP in 2007, the Technovisionary Award from the India Semiconductor Association in 2007 and the Semiconductor Industry Association Researcher of the Year Award in 2012. He is listed by ISI as one of the 250 Highly Cited Authors in his field.

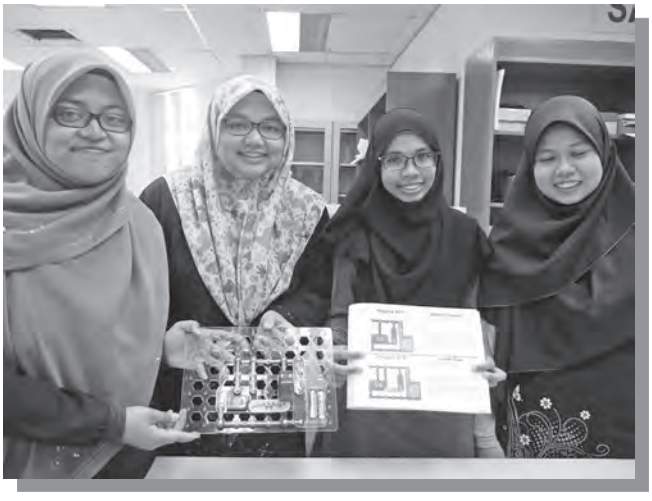
Abstract

Modern electronics has advanced at a tremendous pace over the course of the last half century primarily due to enhanced performance of MOS transistors due to dimension scaling, introduction of new materials and novel device structures. However, while this has enhanced the transistor performance, the opposite is true for the copper interconnects that link these transistors. Looking into the future the relentless scaling paradigm is threatened by the limits of copper/low-k interconnects, including excessive power dissipation, insufficient communication bandwidth, and signal latency for both off-chip and on-chip applications. Many of these obstacles stem from the physical limitations of copper/low-k electrical wires, namely the increase in copper resistivity, as wire dimensions and grain size become comparable to the bulk mean free path of electrons in copper and the dielectric capacitance. Thus, it is imperative to examine alternate interconnect schemes and explore possible advantages of novel potential candidates. This talk will address effects of scaling on the performance of Cu/low-k interconnects, alternate interconnect schemes: carbon nanotubes (CNT), graphene, optical interconnect, three-dimensional (3-D) integration and heterogeneous integration of these technologies on the silicon platform. Performance comparison of these technologies with Cu/low-k interconnects will be discussed.

EDS-ETC Program at IIUM Malaysia

The IEEE ED Malaysia Chapter received the EDS-ETC kits in 2015, courtesy of M. K. Radhakrishnan, Vice President and Fernando Guarin, President-Elect of IEEE EDS. Recently, we conducted two EDS-ETC Train-the-Trainer events at the Kulliyyah of Engineering, International Islamic University Malaysia (IIUM) on February 16th graduate and March 11, 2017, where a total of 28 and 22 undergraduate students participated in the event respectively. The students' feedback were positive in that they could understand the basic theory by constructing simple electronic circuits. These students will assist EDS Malaysia for deploying the EDS-ETC program in local schools.

~P Susthitha Menon, Editor



Participants of EDS-ETC Train-the-Trainer Session at IIUM

Chapter News

MQs, DLs and Conference Reports

Report from Region 9 Subcommittee for Regions & Chapters

By Jacobus Swart

The University of Campinas in Brazil yearly offers a hands-on summer (February in our southern hemisphere) course on semiconductor microfabrication. The course has been offered since 1999 to students from other universities and/or professionals that have no access to cleanroom facilities. The course takes two complete weeks with 8 hours of activities per day. It is about (30%) class instruction, (40%) MOS IC fabrication work in a cleanroom, (30%) process control, characterization measurements, device and circuits testing and CAD simulations. Each group of three students processes two wafers starting with bare wafers to the completion of the MOS devices and a circuit test chip. We believe that this hands-on experience is unique for the participants and provides a much better understanding of concepts, fabrication and devices.

(left to right) Sergio Martinez (student), Jacobus Swart (creator of the course), Prof. José Diniz (coordinator of the course) and Christian Torres (student) in front of the entrance of the clean room microfabrication lab

In 2017, we could once again offer partial EDS fellowships to support two students from Region 9 to disseminate this experience, contributing to the interchange of students within the region and providing a tangible benefit of EDS membership. Two students from Colombian universities were selected to participate this year. The following are some of the comments from the selected students:

Sergio Martinez (U. Javeriana, Bogota): *"We could take advantage of this incredible experience, thanks to the help and guidance throughout the course, the instructors shared their extensive and deep knowledge in this area (semiconductor fabrication process) that for me was completely new. It was unique sharing seminarium and labs with both, great professors and great classmates. I now have a deeper understanding of how interesting, complex and multidisciplinary the field of electronics is. It requires knowledge and advances in fields like chemistry, and physics. From the course I really enjoyed the whole experience, because the explanations gave me a deeper understanding of the parameters that describe a device model, and the ability to prove the concepts in the laboratories was remarkable."*

Christian Torres (Universidad Industrial de Santander, Bucaramanaga): *"It was a great experience for a circuit designer to implement from raw materials discrete transistors and circuits. Even though we were not using the latest technology nodes, the ability to reinforce fabrication, simulation and practice was tremendous. We never had exposure to tools like Ion implanters nor FIB and have the ability to manipulate nanostructures like tubes and graphene films. After this course I now have the certainty that microelectronics is one of the most integral and complete of the applied sciences. I hope to be able to take back with me some of the devices we have fabricated to share with my classmates."*

~Joao Antonio Martino, Editor

Conferences Organized by the AP/MTT/ED/AES/ GRS/NPS East Ukraine Chapter

This year, as usual, our Chapter co-organized and co-sponsored the following IEEE meetings:

- **IEEE International Conference on Electronics and Nanotechnology (ELNANO 2017)**, April 18–20, 2017, at the National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute" (NTUU-KPI) in Kyiv, Ukraine.

This event brings together researchers from the areas of nanotechnology, biomedical electronics, signal processing, power electronics, smart grids, and electronic systems from leading universities, research labs and industry.

- **2017 IEEE Ukraine Conference on Electrical and Computer Engineering (UKRCON-2017)**, May 29–June 2, 2017. The UKRCON general theme, **Celebrating 25 Years of IEEE Ukraine Section**, reflects the profound impact of IEEE on the Ukrainian scientific community. The IEEE Ukraine Section was founded on November 21, 1991, and for 25 years has been helping Ukrainian scientists find ways to collaborate with various international partners through IEEE conferences and grants. The UKRCON-2017 venue will be NTUU-KPI in Kyiv, Ukraine.
- **IEEE Milestone Plaque "L-Band Radar Zenith, 1938" Unveiling Ceremony**, Kharkiv, Ukraine. Pulsed decimeter-wavelength radar was developed and tested in 1938 in Kharkiv by the scientists of the Laboratory of Electromagnetic Oscillations of the Ukrainian Institute of Physics and Technology, established there in 1929. This milestone was recently approved by the IEEE Board of Directors, and an official dedication ceremony is tentatively scheduled for the beginning of June 2017, just after the IEEE UKRCON-2017 in Kiev. This will be the first IEEE milestone in Ukraine and we believe that its impact will be felt in this country for many years ahead.
- **Workshop on Millimeter and Sub-Millimeter Wave Technologies and Equipment for the Permittivity Measurements of High-Loss Materials** (full-day event, tentatively scheduled for August 2017).

The workshop is viewed as a platform for sharing knowledge and experience between the professionals in the area of RF/Microwave applications including wave propagation, radiation sources, interaction with materials, permittivity measurements, biomedical sensing, modeling approaches, and design and construction of microwave devices. This workshop will give an overview of actual "hot topics" relevant to its scope and will include several talks by invited speakers and active interaction between the speakers and the attendees.

- **International Young Scientists Forum on Applied Physics and Engineering (YSF 2017)**, October 17–20, 2017, in Lviv, Ukraine.

This is the third event for young professionals and students from Ukraine and abroad. The first YSF was held in 2015 at the Dnipro National University and in cooperation with young scientist conference "Problems of Theoretical Physics" of the Institute for Theoretical Physics of the National Academy of Sciences of Ukraine (NASU). YSF-2016 was held in Kharkiv and hosted by the National Technical University "Kharkiv Polytechnic Institute." This year's YSF venue will be in Lviv, the largest city in Western Ukraine that is one of the main cultural centers of the country.

Several times a year our Chapter holds technical meetings with themed presentations at the O. Y. Usikov Institute for Radiophysics and Electronics NASU in Kharkiv. These meetings cover topics concerning all aspects of engineering, physics, theory, experiment and simulation of electron devices, semiconductors, metals, plasmas, etc. We expect to hold at least 12 such meetings during this year.

Prof. Nikolay Cherpak
Chapter Chairman

Dr. Vitalii Shcherbinin
Chapter Vice-chair

Dr. Kateryna Arkhypova
Chapter Secretary
Kharkiv, Ukraine

~Daniel Tomaszewski, Editor

IEEE EDS Mini-Colloquium
Events Organized in India

ED Mini Colloquium at ED Meghnad Saha Institute of Technology Student Branch Chapter

–by Manash Chanda and Swapnadip De

The ED Meghnad Saha Institute of Technology (MSIT) Student Branch Chapter, IEEE MSIT Student Branch and ED Kolkata Chapter, in association with the Department of ECE, MSIT jointly organized the IEEE EDS Mini Colloquium on "Nano-Scale Device and Circuit Design" on Saturday, March 25, 2017 at MSIT. The one-day program featured three IEEE EDS Distinguished Lecturers: Prof. C. K. Sarkar, Professor of Jadavpur University, Dr. Manoj Saxena, Associate Professor of Deen Dayal Upadhyaya College, University of Delhi and IEEE EDS DL, Prof. G. N. Dash, Professor of Electron Devices Group, School of Physics, Sambalpur University, and Prof. Ajit Kumar Panda, Professor of NIST Berhampur. The first half of the program consisted of two DL talks titled *"Universal Sensor Interfacing Circuit Design, Fabrication and Characterization: A case study"* and *"Embedded Insulator Based Novel Nanoscaled Novel MOSFET Structures"* by Profs. Ajit Kumar Panda and Manoj Saxena respectively. Prof. Saxena also highlighted the benefits of EDS membership. The second session consisted of DLs titled *"Versatility of GaN-based Heterostructure Nanotransistors"* and *"Prospects and Challenges of Graphene FETs"* by Prof. C. K. Sarkar and Prof. G. N. Dash, respectively. The program attended by 90 participants, consisted of undergraduate and postgraduate students from different engineering colleges and universities of the region.

Attendees and DLs during the Mini-Colloquium at MSIT

IEEE EDS Mini Colloquium at ED NIST Student Chapter, Berhampur

–by Ajit Kumar Panda

The ED NIST Student Chapter organized the 7th IEEE EDS Mini-Colloquium on "Quantum Devices" on March 6, 2017, at National Institute of Science & Technology, Palur Hill, Berhampur, India. Dr. Subir Sakar talked on low power architectures, Prof. G. N. Dash highlighted the Graphene FET, Prof. C. K. Sarkar discussed about versatility of GaN-Based hetero structure nano Transistors and Prof. Manoj Saxena talked about Dielectric Pocket MOSFET: A Novel Device Architecture. The mini-colloquium was attended by 81 participants, including faculties and M.Tech students.

~Manoj Saxena, Editor

Participants of Quantum Devices mini-colloquium on March 6th

IEEE EDS Mini-Colloquium on Semiconductor Device Technologies & Compact Modeling in Barcelona

On Tuesday, February 7, 2017, The Electron Devices Society organized a mini-colloquium linked to the 11th Spanish Conference on Electron Devices (CDE), which was held in Barcelona from February 8–10, 2017. The Chairs of the mini-colloquium were Prof. Lluís F. Marsal (Chair of the ED Spain Chapter) and Prof. Benjamin Iñiguez, both from Universitat Rovira i Virgili (URV), Tarragona, Spain. Four invited speakers, all of them EDS Distinguished Lecturer, conducted talks ranging from semiconductor device technologies to compact modeling.

Prof. J.-H. He, from the King Abdullah University of Science and Technology, Saudi Arabia made a presentation entitled "Flexible, Foldable and Multi-Functional Paper-Based Electronics." Prof. E. Miranda, from the Autonomous University of Barcelona (UAB) targeted the compact modeling of hysteresis effects in RRAM devices. Prof. B. Iñiguez (URV, Spain) addressed the compact modeling and parameter extraction of Amorphous Oxide TFTs. Finally, Prof L. F. Marsal (URV, Spain) gave a talk entitled "Fabrication of nanostructured polymers for organic solar cells."

Lluis F. Marsal
Universitat Rovira i Virgili
Tarragona, Spain

~Jan Vobecky, Editor

Important Information When Planning Your Next EDS Chapter Event

Dear EDS Chapters:

When planning your upcoming chapter meetings, workshops, etc., please remember to visit the EDS website for a recent list of EDS Distinguished Lecturers and lecture topics.

✓Checklist

- Chapter contacts EDS DL to check availability, confirms date/location of lecture, discusses DL funding needs and determines chapter funding
- EDS DL completes EDS DL Activity Log and Funding Request Form
- If applicable, obtain EDS funding approval
- Chapter publicizes lecture via web, email, etc. Obtain a chapter member list via SAMIEEE (http://www.ieee.org/about/volunteers/samieee/index)
- If applicable, DL submits an IEEE expense report to Laura Riello, to receive reimbursement
- Chapter Chair/DL Coordinator submits an EDS DL/MQ Feedback Form

If you have any questions and/or need more information, please do not hesitate to contact Laura Riello, EDS Executive Office.

Thank you for your continued support of the Society.

Your Chapter Could Be Missing Important Notices and Funding Opportunities!

Please remember, whenever there is a change to Chapter Officers, both IEEE and EDS must be notified. Please follow these two steps:

1) Report officer changes to IEEE via the vTools Officer Reporting form: https://officers.vtools.ieee.org/ *(access to vTools requires use of an IEEE account)*.
2) Report officer changes to EDS by completing the Chapter Chair Update Form: https://ieeeforms.wufoo.com/forms/pgu6n1i1ixepnu/

Thank you in advance for your assistance.

Regional News

USA, Canada & Latin America (Regions 1–6, 7 & 9)

ED/SSC Argentina Chapter
–by Felix Palumbo

Albert Wang, IEEE Fellow and Professor of Electrical and Computer Engineering at University of California, recently visited the ED/SSC Argentina Chapter. The program was held at National Technological University in Buenos Aires, Argentina (FRBA-UTN), February 20, 2017. The meeting comprised of meeting in the Nanoelectronics laboratory with PhD students and EDS members. An IEEE EDS Distinguished Lecture was held in the afternoon, entitled *"EDS protection Design for IC and systems."*

After the talk, the Prof. Wang and Prof. Palumbo (EDS member and organizer of the activity), discussed with the attendees about possible collaboration between IEEE chapters, encouraging young people to participate in EDS activities.

~Joao Antonio Martino, Editor

Prof. Albert Wang during his lecture at National Technological University in Buenos Aires, Argentina (FRBA-UTN)

Prof. Albert Wang (first on the left), the organizer Felix Palumbo and the other participants

Europe, Middle East & Africa (Region 8)

MTT/ED/AP/CPMT/SSC West Ukraine Chapter and LPNU ED Student Branch Chapter
–by Mykhaylo Andriychuk and Ihor Zhuk

The IEEE MTT/ED/AP/CPMT/SSC West Ukraine Chapter together with the Lviv Polytechnic Electron Devices Society Student Branch Chapter co-organized the 14th International Conference on the Experience of Designing and Application of CAD Systems in Microelectronics (CADSM-2017). The Conference was held at the Polana-Svalava resort in the Carpathian Mountains, during February 21–25, 2017. It was organized under the auspices of the Ministry of Science and Education of Ukraine and Lviv Polytechnic National University. The conference technical program consisted of the honorary plenary invited session and eight oral sessions devoted to the topics:

- Modeling and Optimization for Technological Processes
- Models and Methods for Radioelectronics Device and System Design
- Design of Specialized Systems and Devices
- CAD Modern Information Technology
- Models and Methods for Microelectromechanical Systems
- Technologies for Medicine—Biomedical Electronics

One hundred eighteen reports by 347 authors from Austria, France, Iraq, Poland, Russia, Sweden, Vietnam, and Ukraine were presented.

The conference opened with an interesting historical overview devoted to previous CADSM issues. Prof. Mykhaylo Lobur, Conference

Active discussions at the CADSM-2017 poster session

Chairman, acquainted the audience with highlights of the main achievements of the conference, beginning with CADSM-2001, which was the first conference in Ukraine to receive technical co-sponsorship from the IEEE Electron Devices Society. CADSM remains one of the leading conferences organized in Ukraine and in Eastern Europe which is devoted to the problems of microelectronics, IC technologies, and specialized CAD software.

The invited talks were devoted to the novel trends in microelectronics technology, to interaction of the electromagnetic field of the different nature with the microelectronic devices, to design of microelectromechanical systems, and application of microelectronics in medical research.

The most interesting presentations, which stimulated active discussions during the plenary session and discussions in the lobby, were the following:

- "ASICs Design for Space Applications and Research of Related Thermal and Electro-Magnetic Phenomena" – by Prof. Andrzej Napieralski, Lodz, Poland.
  The author discussed the role of Department of Microelectronics and Computer Science (DMCS) in design of the first Polish ASIC for space applications, and introduced research projects focused on analysis of the most important phenomena in this area and their novel mathematical description demanded by modern deep submicron semiconductor processes.
- "Method of Finite-Element Mesh Repositioning for FSI Modeling of Living Cell Behavior in Microfluidics" –by Danylo Lizanets, Oleh Matviykiv, Oleksandr Halushko, Wroclaw, Poland / Lviv, Ukraine;
  The presentation was devoted to approaches and algorithms for fluid mesh rotation in mechanical models of a living cell. Described algorithms were designed to prevent the FEM mesh from twisting and self-intersection in numerical simulations of a rotating fluid mesh. These algorithms provide means for modeling a wider range of solid and shell rotations.
- "RLC-Circuit Reduction Algorithm Modifications" – by Oleksiy Chkalov, Oleksandr Beznosyk, Oleksii Finogenov, Tatiana Ladogubets, Kharkiv, Ukraine;
  The presentation discussed novel algorithms decreasing the reduction time and memory consumed. Reduced RLC circuit's design procedures were also discussed.
- "FEM Analysis of a 3D Model of a Capacitive Surface-micromachined Accelerometer" – by Michal Szermer, Jacek Nazdrowicz, Wojciech Zabierowski, Lodz, Poland;
  The presentation was devoted to analysis of a 3D model of a surface-micromachined accelerometer. Using the COMSOL Multiphysics software, the basic mechanical parameters, which give the information about mechanical properties of the modeled sensor, were determined.
- "Mathematical Models of Informative Characteristic of Tissues in Surgical Wound at Monitoring the Recurrent Laryngeal Nerve by Electrophysiological Method" – by Mykola Dyvak, Andriy Pukas, Natalia Padletska, Viktor Shidlovsky, Andriy Dyvak, Ternopil, Ukraine.
  The new electrophysiological methods and adopted microelectromechanical tools for identification of the recurrent laryngeal nerve were reported.

Traditionally, the young scientists and students were recognized for

the best presentations at the conference. This year, they were granted free IEEE and EDS membership subscriptions for 2017.

The high professional level of the conference, its friendly atmosphere and great hospitality of the organizers are the reasons why everyone who attended the CADSM before, will almost certainly come again. The Organizing Committee welcomes old and new participants to the CADSM-2019.

~Daniel Tomaszewski, Editor

Student presenters who won the 16th IEEE EDS Kansai Chapter MSFK Award and the IEEE EDS Kansai Chapter of the Year Award

Asia & Pacific (Region 10)

ED Kansai Chapter

–by Michinori Nishihara

The ED Kansai chapter hosted the 16th annual Kansai Colloquium Electron Devices Workshop on January 30, 2017, at OIT UMEKITA Knowledge Center, Osaka, Japan. The event attracted 28 participants including 21 IEEE members and authors from the Kansai area who presented 8 excellent papers. The papers were specially selected from (1) major conferences such as IEDM or SSDM and (2) technical papers on electron devices published during the past 12 months.

The program was divided into three sections as follows: (1) Sensor, Solar Cell, and Emerging Devices, (2) Power and Compound Semiconductor Devices, and (3) CMOS Process, Device, and Circuit.

The Award Committee selected two papers from student presenters for the 16th IEEE EDS Kansai Chapter MSFK Award. The winners were Dr. Katsuya Kito of Ryukoku University for his paper titled, *"Temperature and Illuminance Detections by Hybrid-type Carrier-generation Sensors using n-type and p-type Poly-Si TFTs"* and Dr. Ryo Kishida of Kyoto Institute of Technology for the paper titled *"Negative Bias Temperature Instability Caused by Plasma Induced Damage in 65 nm Bulk and Silicon on Thin BOX (STOB) Processes"*

The Committee also selected one paper for the IEEE EDS Kansai Chapter of the Year Award. The winning paper was *"Terahertz Emission from Individual Subcells in a Triple Junction Solar Cell Excited by a Wavelength Tunable Pulsed Laser"* by Dr. Shota Hamauchi of Osaka University.

The presented papers were all excellent and stimulated many questions and discussions with the audience, as they were selected from already qualified papers of

Participants of the 16th annual Kansai Colloquium Electron Devices Workshop

major conferences and technical journals. This workshop is playing an important role in encouraging students and young engineers in the industry to extend their technical knowledge and career.

After the technical meeting, we held the annual general meeting to select the new officers for a two-year term and to review activities of ED Kansai in 2016 and to discuss plans for 2017.

~Kuniyuki Kakushima, Editor

Prof. Junning Chen, Prof. Steve Chung (seminar chair), and Prof. Ming Liu (speaker, from IME/CAS

EDS Distinguished Lecture-ED Taipei

–by Steve Chung

The ED Taipei Chapter together with the EDS NCTU student chapter held an invited DL talk on March 28, 2017 by Prof. Ming Liu, the current Chair of IEEE ED Beijing Chapter, and from the Institute of Microelectronics, Chinese Academy of Sciences, China. She gave a talk entitled, "High Performance Selector and 3D Integration for Resistance RAM". She started by introducing the major activities of CAS with collaborations with more than 100 institutions nationwide, in particular she presented the major activities in microelectronics (based in Beijing) with nearly 1,000 employees and more than 400 Master/Ph.D. students working together in a wide areas of microelectronics. Then, she presented their works published in IEDM and the VLSI Symposium on the study of Vertical RRAM in a 3D crossbar structure. In particular, she presented developments on high performance selector and 3D integration that can be projected to a 5 nm dimension. The 3D vertical RRAM (V-RRAM) provides a cost-effective approach for high density integration. However, the development of V-RRAM has been impeded by lack of a high performance self-selective cell (SSC). Unlike 3D stacked cross-point arrays, an individual selector is not allowed in V-RRAM. The self-selective cell is the only choice to prevent leaking current in the 3D V-RRAM crossbar array. This talk was attended by approximately 20 graduate students, professors, and postdoctoral researchers.

There are also several upcoming conferences, including: 2017 VLSI-TSA, April 24–27, 2017, http://expo.itri.org.tw/2017vlsitsa, 2017 IEEE ISNE (International Symposium on Next Generation Electronics), May 23–25, 2017, at National Taiwan Ocean University, https://isne2017.ntou.edu.tw/; IEEE EDSSC (International Conference on Electron Devices and Solid-State Circuits), October 18–20, 2017 at National Tsing Hua University, http://www2.ess.nthu.edu.tw/edssc2017/, with IEEE EDS as a co-sponsor and key members of the local chapter are involved. The paper submission date for 2017 ISNE is May 7, 2017. Please make a note on your calendar for paper submission and attending the conference.

EDS Distinguished Lecture-ED Nanjing Chapter

–by Weifeng Sun

Distinguished Lectures were sponsored by IEEE EDS and were organized by the School of Electronic Science and Engineering, Nanjing University, March 14, 2017. The event was held to exchange the latest ideas and promote the research and development on nanoelectronic devices, sensor and microelectronics-system integration, and CMOS applications.

The lecture was held in Conference Room One of the School of Electronic Science and Engineering at 14:30–17:30 pm. Professor Kunji Chen presided. Professor Hiroshi Iwai made a keynote speech on the Scaling Theory for Nanoelectronic Devices and the World. Afterwards, Professor Edward Yi Chang made a keynote speech on InGaAs MOS Devices for Post-Si COMS

Prof. Hiroshi Iwai, Professor Kunji Chen, Professor Edward Yi Chang, Professor Stella Kuei-Ann Wen and some other members of the Chapter after the talk

Applications and Professor Stella Kuei-Ann Wen made a keynote speech on Sensor and Microelectronics-system Integration for Life Enhancement.

EDS Distinguished Lecture-ED Xi'an Chapter

–by Hongliang Lu

On March 15, 2017, Yic Huang and Yonggang Zheng, presented talks at the Lectures Series on Advanced Technology in Integrated Circuits held by the ED Xi'an Chapter at Xidian University, Xi'an, Shaanxi, China. More than 100 students from the School of Microelectronics experienced their excellent talks.

In recent years, China's imports of electronic components (including ASIC) has exceeded oil to become the first major commodity import. The country is also strongly supporting the development of the Integrated Circuits industry. That is why two advance managers were invited to lecture in this series. In Huang's talk, he presented a brief introduction on low power technology in circuits design. Meanwhile, in Zheng's talk, he gave us an overview on the SoC design and manufacturing process and the design trends and challenges on the latest Ultra Large SoC projects.

~Ming Liu, Editor

ED Malaysia Kuala Lumpur Chapter

–by M. R. Aliza Aini, S. Noorjannah Ibrahim and A. B. Rosminazuin

Annual General Meeting 2017

The ED Malaysia Chapter 27th Annual General Meeting (AGM) and Silver Jubilee Celebration were held January 13. 2017, at the Putrajaya Marriott Hotel, Putrajaya. The AGM was held to table EDS events and financial activities in 2016 among EDS members. Thirty-one members from the ED Malaysia Chapter attended the AGM. New executive committees were elected and Dr. P. Susthitha Menon was elected to lead the ED Malaysia Chapter for the year 2017–2018. Also, the 25th Anniversary of the IEEE Electron Devices (ED) Malaysia Chapter was organized to show appreciation for all the contributions and hard work by past chairs, executive committees, and members. At the event, ED advisor, Dr. Burhanuddin Yeop Majlis, delivered a speech on the history of the chapter. The event included a video which featured EDS history, past chapter chairs, awards won by the chapter and members, as well as memorable moments from conferences. The event concluded with an award ceremony to appreciate all past chairs.

Attendees of the EDS Malaysia AGM 2017

IEEE Senior Member Elevation Workshop

The Electron Devices Society established the EDS Senior Member Program to both complement and enhance the IEEE's Nominate-a-Senior-Member Initiative and make IEEE/EDS members aware of the opportunity and encourage them to elevate their IEEE membership grade to Senior Member. In view of this, EDS Malaysia Chapter and IEEE Malaysia Section conducted the IEEE Senior Member Elevation Workshop on 14 March 2017 at Multimedia University (MMU). It was co-organized with the Center for Advanced Devices and Systems (CADS), Faculty of Engineering, MMU. 15 participants attended the workshop hailing from MMU, UKM, AIMST and Taylor's University Malaysia. An overview about EDS and the Senior Member benefits were given by Drs. Susi and Faizal, respectively. The participants' feedback were positive and inspired them to apply for senior membership. Three

A group photo of the IEEE Senior Member Elevation Workshop at MMU

EDS Malaysia excom, Dr. Zubaida, Dr. Noorjannah and Dr. Haslina, successfully submitted their IEEE senior member application citing EDS as the nominating entity.

2017 IEEE Regional Symposium on Micro and Nanoelectronics (RSM)

IEEE ED Malaysia Chapter is pleased to invite all to Penang Island, Malaysia (nicknamed as "*Pearl of the Orient*" and is a UNESCO World Heritage Site) for the 11th IEEE Regional Symposium on Micro and Nanoelectronics (RSM) 2017, which will be held from August 23–25, 2017. Since 1997, this bi-annual technical conference aims at bringing together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics. The conference is organized by the EDS Malaysia and technically co-sponsored by the IEEE Malaysia Section. Over the last twenty years, the RSM conference series has become the prominent international forum on semiconductor electronics embracing all aspects of the semiconductor technology from circuit device, modeling and simulation, photonics and sensor technology, MEMS technology, process and fabrication, packaging technology and manufacturing, failure analysis and reliability, material and devices and nanoelectronics. EDS DL and R10 SRC Chair, Professor Ru Huang from Peking University, China will be one of the keynote speakers. For further information, please visit the conference website *http://ieeemalaysia-eds.org/rsm2017/.*

~P Susthitha Menon, Editor

ED NIST Student Chapter

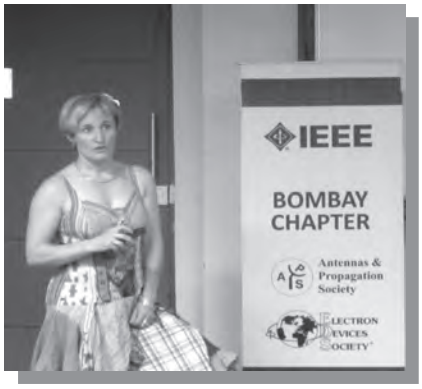
–by Ajit K. Panda

The ED NIST Student Chapter organized the 3RD National Conference on Devices and Circuits (NCDC-2017) on March 7, 2017, at the National Institute of Science & Technology, Palur Hill, and Berhampur, which was attended by over 80 students and faculty members. A total of 32 papers were accepted for publication in the conference proceedings. The paper entitled "SAR Logic Design for Successive Approximation ADC for Biomedical Applications," was awarded as best paper by the session chairs.

AP/ED Bombay Chapter

–by Anil Kottantharayil

The AP/ED Bombay Chapter organized seven talks during January–March 2017, and were attended by students, research staff and faculty of IIT Bombay. Students and faculty members from educational institutions in and around Mumbai, and researchers and engineers from several Mumbai area companies also attended. Prof. John R. Reynolds from Georgia Institute of Technology, USA, in his talk titled, *"Conjugated Polymers in Active Devices: Photovoltaics, Electrochromism and Charge Storage as Case Studies,"* addressed the synthesis and optimization of the morphology of solution processed π-conjugated oligomers and polymers, as they are applied in organic electronic devices. Dr. Vincent Huard from ST Microelectronics Crolles, France, presented his talk titled, *"Enabling Critical Systems in advanced CMOS nodes,"* where he reviewed the reliability challenges in future critical systems that are designed in advanced CMOS nodes. Dr. Sourabh Dongaonkar, Intel, Hillsboro, Oregon, USA, in his talk titled, *"Transistor Variation on Industrial Scale: Measurement and Analysis on Intel 14 nm Logic FinFET Technology,"* emphasized that in hyper-scaled technologies, accurate and high volume measurement and analysis of threshold voltage variation in transistors and temporal Vth variation due to noise are fundamentally important for process development. Prof. Masaki Mizuguchi, Tohoku University, Japan, in his talk titled, *"Spin caloritronics in ordered alloy materials,"* focused on the recently established spin caloritronics field of research. He explained his research group's study on the correlation between magnetic anisotropy and the ANE in various materials. The enhancement effect of ANE with spin-wave spin currents in nanostructures was also discussed with theoretical viewpoints. Prof. Corinne Dejous, the IMS Bordeaux, France, gave a brief introduction on the IMS Bordeaux



Prof. Corinne Dejous delivering her talk

Dr. Mukta Ghate Farooq (left) with the IIT Bombay faculty members after her lecture

Laboratory at the beginning of her talk and presented an overview of the efforts made at IMS Bordeaux labs on a spectrum of applications of MEMS, in the talk, "*IMS Bordeaux: Wave-based resonant microsensors for (bio)chemical detection, environmental and health related applications.*"

Dr. Mukta Ghate Farooq, IEEE Fellow & Global Foundries Fellow, Global Foundries, USA, in her IEEE EDS Distinguished Lecture titled, *"2.5D / 3 D Integration Technology for CMOS,"* explained that 2.5D/3D integration technology encompasses a wide variety of configurations, which employ TSVs (Through Silicon/Substrate Vias) in a silicon wafer. Prof. Krishna Shenai, IEEE Fellow & Distinguished Lecturer of the IEEE Power Electronics Society and presently with NMAM Institute of Technology, Nitte, Karnataka, in his talk, *"Power Electronics for 21st Century Energy Economy,"* discussed the opportunities and challenges in both silicon and wide bandgap (WBG) power semiconductor devices and their applications in systems.

ED Uttar Pradesh Section – Kanpur Chapter

–by Yogesh Chauhan

The Chapter organized a Global Initiative on Academic Network (GIAN) course on "*High Frequency Device Characterization and Modeling for THz applications,*" from February 27–March, 3, 2017. The GIAN course was conducted by Prof. Thomas Zimmer, Laboratory of the Integration of the Material to the System (IMS), Bordeaux, France. It covered many application-oriented topics related to THz devices including, device modeling, parameter extraction procedure, electrothermal effects and their characterization with pulse DC, AC and RF measurements, next generation THz devices: graphene and 2D-devices, and opportunities, challenges and solutions in THz devices and circuits. More than 50 students from various parts of India participated.

A one-day "*IEEE Workshop on Compact Modeling,*" was organized on March 3, 2017, and inaugurated by the Deputy Director, IIT Kanpur, Prof. Manindra Agrawal. The event was attended by more than 70 IEEE and EDS members from institutes and organizations across India. The workshop began with an informative lecture delivered by the Chair, EDS U.P. Chapter, Dr. Yogesh Singh Chauhan, on the benefits of IEEE and EDS memberships for researchers.

The technical session began with a talk delivered by Dr. Yogesh Singh Chauhan, on *"Industry Standard Compact Modelling."* Then, Mr. H.S. Jattana, SCL, Chandigarh, Mr. Mohit Khanna, Keysight Technologies, Dr.Nihar Ranjan Mohapatra, IIT-Gandhinagar, Dr. Sushant Mittal, Micron Technologies, Prof. Thomas Zimmer, IMS-BORDEAUX, France, Dr. Abhishek Dixit, IIT-Delhi, Dr. Saurabh Lodha, IIT-Bombay, Dr. Manoj Saxena, Delhi University, Dr. Santosh Kumar Vishvakarma, IIT-Indore, Dr.Swaroop Ganguly, IIT-Bombay, and Dr.Sitangshu Bhattacharya, IIIT-Allahabad gave talks on various subjects related to compact modeling of Nano-scale devices. Mr. Sheikh Aamir Ahsan, Mr. Avirup Dasgupta, Mr. Chandan Yadav and Mr. Priyank Rastogi, all from Nano-Lab, IIT Kanpur, presented their work on GaN HEMTs, 2D materials and other topics in the poster session.

The chapter and Department of Electrical Engineering, IIT Kanpur, jointly organized a short-term course on "*Modeling and Simulation of Nano-Transistors,*" February 13–17, 2017. In the technical sessions of the course, lectures were delivered by Dr. Amit Kumar Agarwal, Dr. Amit Verma, Dr. S. Sundar Kumar Iyer, Dr. Aloke Datta, Dr. Y. S. Chauhan, Dr. Somnath Bhowmick, Dr. K. V. Srivastava, Dr.Sudip Ghosh, Mr. Chandan Yadav, and Mr. Sheikh Aamir Ahsan, all from IIT Kanpur. Project funding, proposal writing, and new research topics were

ED Uttar Pradesh Chapter GAIN course on "High Frequency Device Characterization and Modeling for THz applications" and "IEEE Workshop on Compact Modeling"

also covered in the last session. The event was well attended by more than 170 researchers from across India and Bangladesh.

The chapter arranged within the Microelectronics Seminar series an IEEE-EDS lecture on *"Record High Graphene Transistor Performance,"* on January, 10, 2017 by Dr. Mayank Shrivastava from IISc Bangalore.

A Distinguished Lecture on "*CMOS Transistors—Operation, Scaling, Reliability, and the Way Forward,*" by Prof. Souvik Mahapatra, IEEE Fellow and INAE, Department of Electrical Engineering, IIT Bombay, was conducted by the Chapter on February, 20, 2017. Prof. Mahapatra covered the following topics: (i) CMOS transistor operation and conventional scaling, (ii) alternative scaling—innovations in materials and structures, and (iii) reliability - transistor ageing and breakdown. The talk was attended by students from electronics, electrical engineering, physics, and materials science. The speaker also discussed the research opportunities at IIT Bombay in the area of semiconductor devices.

ED Heritage Institute of Technology

–by Atanu Kundu

The Department of Electronics & Communication Engineering, Heritage Institute of Technology hosted a Distinguished Lecture Program by Dr. Meyya Meyyappan, Chief Scientist from NASA, Ames Research Center, California. The event was organized in collaboration with the IEEE Kolkata Section, ED Kolkata Chapter, ED HITK Student Branch Chapter and the SSCS Kolkata Chapter. He delivered a lecture on *"Nanomaterials in Nano electronics and Optoelectronics"* on January 6, 2017, which attracted over 90 attendees.

The Department of Electronics & Communication Engineering, MCKV Institute of Engineering organized a Students' Article Competition "PRAYAS-2017" on February 18, 2017. The event was held at MCKVIE under the sponsorship of IET (UK) Kolkata Local Network, MCKVIE and IEEE SSCS and EDS Kolkata Chapters. Seventeen articles in various domains of Electronics & Communication Engineering and allied fields were accepted for the event. Fifteen articles were presented and a total of twenty-seven participants from various engineering colleges/universities participated.

The Department of Electronics & Communication Engineering, Heritage Institute of Technology hosted a Lecture Program by Prof. Siben Dasgupta, Professor, Wentworth College, USA. The event was organized in collaboration with the ED Kolkata Chapter and the ED HITK Student Branch Chapter. He delivered a lecture on *"Digital Controls,"* March 9, 2017, which attracted more than 40 attendees.

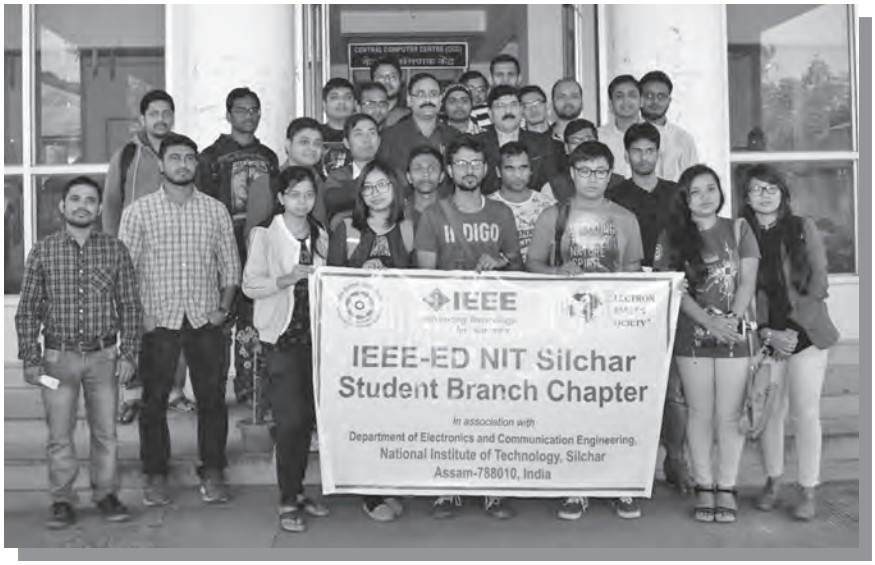
Under the technical co-sponsorship of the IEEE Electron Devices Society Kolkata Chapter, Department of Electronics and Communication Engineering and Department of Computer Application of RCC Institute of Information Technology, jointly organized an International Conference on Computational Science and Engineering from October 4–6, 2016, at CII-Suresh Neotia Centre of Excellence for Leadership, Saltlake. Mr. Joydeep Banerjee (Lead University Relations, IBM) emphasized the need of the product-oriented and outcome-based technical education at the inaugural ceremony. Prof. Atanu Kundu, Chairman, EDS Kolkata Chapter explained the importance of a research-oriented teaching approach for technical enrichment in the opening session.

ED NIT Silchar Student Branch Chapter, Assam, India

–by T R Lenka

Prof. Durga Madhab Misra, Professor at NJIT, USA and IEEE EDS Distinguished Lecturer delivered a talk on January 9, 2017, at the ED NIT Silchar Student Branch Chapter, Assam, India, after completion of Global Initiative of Academic Networks (GIAN) Course on "*Nanoelectronics Challenges for Internet of Things,*" sponsored by MHRD, Govt. of India. In his talk on *Challenges of Nanotechnology,* he emphasized on high–k dielectrics towards applications of

Inaugural ceremony of the program and Dr. Meyya Meyyappan delivering his lecture



Prof. Durgamadhab Misra, EDS Distinguished Lecturer, Dr. T. R. Lenka, Faculty Advisor, Mr. S. R. Routray, Student Chair

Nanoelectronic devices. About 40 participants attended the program.

ED Institute of Engineering & Management Student Branch Chapter

–by Arunabha Ghoshal

The first seminar of the ED Institute of Engineering & Management Student Branch Chapter was held March 14, 2017. The topic of the seminar was *"Semiconductor Devices- The Wonder Element to direct the path of Civilization and Social Life."* Dr. Sanatan Chattopadhyay gave his seminar talk and highlighted the relevance of quantum mechanical effects such as electron tunneling through barriers.

ED/CAS Hyderabad Chapter

–by Mohammed Arifuddin Sohel

The ED/CAS Chapter conducted a panel discussion on career opportunities in the electronics sector at Vasavi Engineering College on December 19, 2016. About 100 students participated. The panelists were Prof. K. Subbarangaiah, Veda IIT, Dr. Govindarajulu, Microsemi, Mr. V. Hanuma Sai, AMS Semiconductors, and Mr. N. Venkatesh, Redpine Signals.

A workshop on E-Health was organized, December 7, 2016, at MJCET. This was a collaborative event of the ED/CAS Hyderabad and ED/CAS Indonesia Chapters. Prof. Soegjiardo, Chapter Chair of ED/CAS Indonesia and Mr. Fabian Hadiatna, Research Scholar from Indonesia, travelled from Indonesia to Hyderabad under the CAS Networking Initiative and presented this workshop. Mr. Joginder Tennikella, CEO of VajraInfratech, was the speaker from the ED/CAS Hyderabad side. About 40 persons attended this workshop.

A one-day workshop on Future of Nanoelectronics was organized by Auroras Scientific, Technical and Research Academy, Bandlaguda on December 21, 2016 at Hotel Katriya Somajiguda, in collaboration with the ED/CAS Chapter of the Hyderabad section. The key speaker for the workshop was Prof. Vijay K Arora, EDS Distinguished Lecturer. The workshop witnessed a participation of over 100 delegates and also included a talk by Mr. MadhavNegi, Membership Development Chair of the IEEE Hyderabad Section.

The ED/CAS Chapter of the IEEE Hyderabad Section organized a two-day workshop on Analog VLSI Design—Bridging gap between Industry and Academia at CBIT, Hyderabad, March 17–18, 2017. The workshop was supported under TEQIP program of Govt. of India. Over 70 students and faculty members attended the workshop, which was aimed at bridging the gap between the classroom design procedures and the desired specifications and limitation of the fabrication industry. Economics governing the design of ICs needs to be known to the designer so that the specifications framed are realizable and circuit performance is reasonable after fabrication. The ESD/EMC issues and their impact on the design were also covered. The highlight of the workshop was that all the speakers were from AMS semiconductors India pvt. Ltd. and provided a complete analog flow from specification to silicon. The speakers were Sri. A.G. Krishna Kanth, Sr. Manager (BL–AOS), Sri. Rohit Ranganathn, Team Leader (Analog), Sri. Ravi Kumar, Senior Engineer (Analog), Sri. Sridhar Setty, Senior Engineer (Analog), AMS Semiconductors India Pvt.

Dr. Sanatan Chattopadhyay delivering his seminar talk and Student Chapter members

Prof. Vijay K. Arora during lecture and attendees of one-day workshop on December 21st

Ltd. The keynote address was delivered by Sri. V. Hanuma Sai, Director, AMS Semiconductors India Pvt. Ltd.

ED Delhi Chapter

–by R. S. Gupta and Sneha Kabra

The ED Delhi Chapter organized a Distinguished Lecture by Prof. Vijay K. Arora, (Professor of Electrical Engineering and Physics Wilkes University), January 13, 2017, at the University of Delhi South Campus. The title of his talk was "*Publish and Flourish Art, Craft, and Sportsmanship of Publishing in Scholarly Journals.*" In this scholarly discourse, the audience walked through the art and craft of taming the mind (attitudes) to train the creative brain in search of solutions to problems, as well as choosing reviewers and journals carefully so that your ideas echo throughout the globe. The talk was attended by about 75 people including students and faculty.

A Distinguished Lecture on *"CMOS Transistors - Operation, Scaling, Reliability and Way Forward"* by Prof. Souvik Mahapatra (Professor, IEEE Fellow Department of Electrical Engineering, IIT Bombay) was organized January 23–24, 2017, at Shaheed Rajguru College of Applied Sciences for Women (Delhi University) and at Deen Dayal Upadhyay College (Delhi University), respectively. The talk was attended by 182 students and faculty from Shaheed Rajguru College of Applied Sciences for Women and 90 students and faculty from Deen Dayal Upadhyay College.

An EDS Distinguished Lecture on *"Microfabricated gas pumps for micro gas chromatography and other applications,"* by Prof. Yogesh B. Gianchandani (Professor, University of Michigan, Ann Arbor), was organized at IIT Delhi, January 25, 2017. The speaker described lithographic manufacturing methods, which may be used for high flow Knudsen pumps. He also described an example of how the architecture of micro gas chromatographs can be adapted to incorporate KPs.

Prof. Souvik Mahapatra along with attendees after the DL, January 23, 2017, at SRCASW

Another IEEE Distinguished Lecture by Dr. Ravinder Dahiya (Reader and EPSRC fellow School of Engineering, University of Glasgow, UK), was organized, March 7, 2017, at IIT Delhi. The title of the talk was *"Large Area Electronic Skin."* The lecture covered recent developments in off-the-shelf sensors and electronic components on flexible printed circuit boards to obtain large area tactile skin for robots and wearable systems and was attended by 35 students and faculty.

The ED Delhi Chapter and Department of Electronic Science, University of Delhi, successfully organized the Second National Conference on Recent Development in Electronics (NCRDE-2017), February 17-18, 2017, at University of Delhi South Campus, New Delhi. The conference was supported by the Department of Science and Technology (DST), Government of India, Defense Research and Development Organization (DRDO) and Society for Microelectronics and VLSI, New Delhi. Eigen Technologies, AGMATEL and Keysight were industry partners of the conference.

The conference aimed to establish an effective platform for institutions and industries to share their ideas, real time experiences and to motivate the work of scientists, engineers, educators and upcoming talent. On February 17, 2017, Dr. R. K. Sharma, Director, Solid State Physics Laboratory, DRDO, Govt. of India, delivered his keynote address highlighting the research and development taking place at SSPL, which was followed by two plenary talks by Prof. Subir Sarkar, Department of Electronics and Telecommunication Engineering, Jadavpur University, Kolkata, and another by Dr. D. S. Rawal, Solid State Physics Lab., DRDO, Govt. of India. Professor Ajit K. Panda, Department of Electronics and Communication, NIST, Berhampur, Odissa, delivered his invited talk on *"Beyond CMOS: HEMT is a prospective device."* Other invited speakers were Dr. Ajay Aggarwal, MEMS and Microsensors Group CSIR-CEERI, Pilani, Dr. V. N. Ojha, Scientist G', CSIR-NPL, New Delhi, Prof. Santanu Mahapatra, Department of Electronic System Engineering., IISc, Bangalore, India, Dr. Amita Gupta, Formerly, Scientist 'G', SSPL, Delhi, Mr. G. Krishna Kumar, Application Engineer, Eigen Technologies Pvt. Ltd., Professor Smriti Shrivastava, Dept. of Instrumentation and Control, NSIT, New Delhi, Dr. Rakesh Vaid, Department of Physics & Electronics, Jammu University, India, Prof. Ashok Mittal, Ex Principal, Ambedkar Institute of Advanced Communication Technologies & Research, Delhi, and Dr. Malay Ranjan Tripathy, Dept. of ECE, Amity University, Noida. The conference had eight technical sessions covering Device Modeling and Simulation, Green Electronics, Nanomaterial and Energy Harvesting, MEMS/NEMS/Sensors, Embedded System, Electronic Circuit/VLSI Design, Antenna/Microwave Technologies and Mobile and Communication Systems.

On February 17, 2017, a one-day short course on *"Design and RF Characterization of GaN High Power Devices and amplifiers,"* was organized in conjunction with the conference. The speakers for the short course were from Solid State Physical Laboratory (SSPL), GAETEC Hyderabad and Industry. Dr. Seema Vinayak, Scientist G, MMIC Division, SSPL, DRDO, Govt. of India, gave opening remarks on the present status of GaN Technology, Dr. Karun Rawat, Dept. of ECE, IIT-Roorkee, delivered a talk on *"Design methodologies of power amplifiers,"* Dr. Sandeep Chaturvedi, GAETEC Hyderabad, explained the concepts of RF Characterisation of GaN High power devices and circuits, Power Combining Techniques were explained by Mr. Umakan Goyal, Scientist-E, MMIC Divison, SSPL, Dr. Meena Mishra, Scientist G, MMIC Division, SSPL, enlightened the audience on Reliability issues in High power devices and Mr. Vishal Gupta, Segment and Team Lead, Sr. Applications Specialist (RF/MW) at Keysight Technologies, explained the upcoming area of X parameters and Non-Linear Device Characterization.

On February 16, 2017, a special session for the undergraduate students was also arranged to encourage research at the undergraduate level. Twenty-one B. Tech projects were presented by final year students of B. Tech Electronics/Instrumentation from different colleges of the University of Delhi. Mr. Dhananjay V. Gadre, Associate Professor, ECE Division, Coordinator, Centre for Electronics Design and Technology, Director, TI Centre for Embedded Product Design, Netaji Subhas Institute of Technology, New Delhi, gave an invited talk on *"Embedded Systems as Core Component in ESDM and Make in India."*

~Manoj Saxena, Editor

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

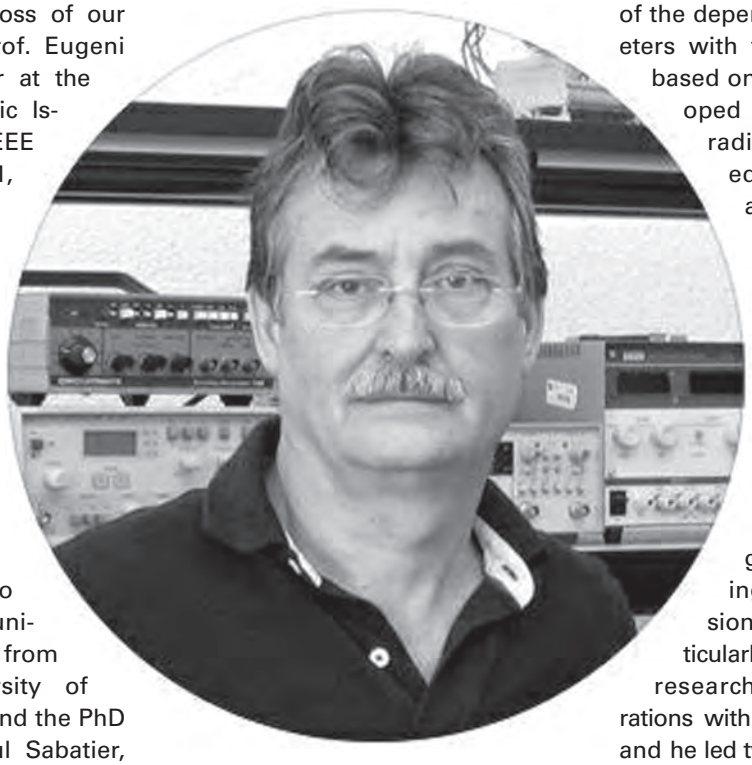
2017 24th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	04 Jul–07 Jul 2017	Ryukoku University Avanti Kyoto Hall 31 Nishi Sanno-cho Higashi Kujo, Minami-ku Kyoto, Japan
2017 IEEE 24th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)	04 Jul–07 Jul 2017	Intercontinental No.1700,Tianfu Road North,High-tech Zone,Chengdu Chengdu, China
2017 30th International Vacuum Nanoelectronics Conference (IVNC)	10 Jul–14 Jul 2017	Herzogssaal Regensburg Domplatz 3 Regensburg, Germany
2017 International conference on Microelectronic Devices, Circuits and Systems (ICMDCS)	10 Aug–12 Aug 2017	VIT University Vellore Vellore, India
2017 32nd Symposium on Microelectronics Technology and Devices (SBMicro)	28 Aug–01 Sep 2017	Gran Marquise Hotel Avenida Beira Mar, 3980 Fortaleza - CE, Brazil
2017 17th Non-Volatile Memory Technology Symposium (NVMTS)	30 Aug–01 Sep 2017	Super C, RWTH Aachen RWTH Aachen Templergraben 57 Aachen, Germany
2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	07 Sep–09 Sep 2017	Kamakura Prince Hotel 1-2-18 Shichirigahama-higashi Kamakura Kanagawa, Japan
2017 39th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)	10 Sep–14 Sep 2017	Westin La Paloma Tucson, AZ, USA
ESSDERC 2017 - 47th IEEE European Solid-State Device Research Conference (ESSDERC)	11 Sep–14 Sep 2017	KU Leuven Campus Social Sciences Leuven, Belgium
2017 Joint International Symposium on e-Manufacturing and Design Collaboration (eMDC) & Semiconductor Manufacturing (ISSM)	15 Sep–15 Sep 2017	The Ambassador Hotel, Hsinchu, Taiwan
2017 XXIInd International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED)	25 Sep–28 Sep 2017	OLes Honchar Dnipropetrovsk National University 72 Haharina Ave. Dnipro, Ukraine

2017 12th European Microwave Integrated Circuits Conference (EuMIC)	08 Oct–10 Oct 2017	NÜRNBERG CONVENTION CENTER (NCC) Messezentrum, NCC Ost Nuremberg, Germany
2017 IEEE International Integrated Reliability Workshop (IIRW)	08 Oct–12 Oct 2017	Stanford Sierra Conference Center 130 Fallen Leaf Road South Lake Tahoe, CA, USA
2017 International Semiconductor Conference (CAS)	11 Oct–14 Oct 2017	Rina Sinaia Hotel 8, Carol I Str. Sinaia, Romania
2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	16 Oct–19 Oct 2017	Hyatt Regency San Francisco Airport 1333 Bayshore Highway Burlingame, CA, USA
2017 Fifth Berkeley Symposium on Energy Efficient Electronic Systems & Steep Transistors Workshop (E3S)	19 Oct–20 Oct 2017	University of California, Berkeley Sutardja Dai Hall Banatao Auditorium Berkeley, CA, USA
2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM	19 Oct–21 Oct 2017	Marriott Biscayne Bay 1633 N Bayshore Dr Miami, FL, USA
2017 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)	22 Oct–25 Oct 2017	Miami Marriott Biscayne Bay 1633 N. Bayshore Drive Miami, FL, USA
2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)	30 Oct–01 Nov 2017	Hyatt Regency Tamaya Resort 1300 Tuyuna Trail Santa Ana Pueblo, NM, USA
2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	12 Nov–16 Nov 2017	Irvine Marriott 18000 Von Karman Ave. Irvine, CA, USA
2017 IEEE International Electron Devices Meeting (IEDM)	04 Dec–06 Dec 2017	Hilton San Francisco Union Square San Francisco, CA, USA
2017 IEEE 48th Semiconductor Interface Specialists Conference (SISC)	06 Dec–09 Dec 2017	Bahia Resort Hotel San Diego, CA, U

In Remembrance of Eugeni Garcia-Moreno

By Benjamin Iñiguez

"We deeply regret the loss of our friend and colleague Prof. Eugeni García-Moreno, Professor at the University of the Balearic Islands (UIB, Spain), IEEE EDS Member since 1991, and Senior Member since 2004. He also served as IEEE EDS Distinguished Lecturer for several years. He was a well-recognized researcher in semiconductor device compact modeling, radiation effects in devices/circuits, and CMOS circuits radiation sensor design.



Eugeni García Moreno obtained the Telecommunication Engineer Degree from the Polytechnic University of Catalonia (UPC) in 1976 and the PhD from the Université Paul Sabatier, Toulouse (France) in 1979. Between 1980 and 1991, he worked as Associate Professor in the Electronics Department of UPC. In 1991, he was a visiting professor at IMEC (Belgium). Since 1992, he was a Full Professor in the Physics Department of the University of the Balearic Islands (UIB), leading the Electronic Technology Group.

He also wanted to be involved in the governance of his university and on research policies. He was Vice-Rector of International Cooperation and of Research and Scientific Policy. Between 2003 and 2004 he was the Director of Research, Innovation and Technological Development of Balearic Islands.

His research focused semiconductor device modelling, the study of radiation effects in semiconductor devices and CMOS circuits, the design of radiation sensors, and the test of integrated circuits. He made very important contributions in these fields. He developed or led the development of analytical and compact models for advanced semiconductor devices, including some of the first explicit DC/AC models for submicron MOSFETs. He was particularly involved in the study and identification of radiation effects on electronic and photonic devices and CMOS circuits, developing models of the dependence of device parameters with the radiation dose, and based on these results, he developed several generations of radiation sensors integrated in CMOS circuits. He authored or co-authored more than 40 journal papers in these topics.

He was an enthusiastic researcher and teacher, and very encouraging as PhD supervisor. He not only provided scientific supervision to his PhD students, but also he gave them useful training in research and professional leadership. He was particularly involved in establishing research and training collaborations with Latin American groups, and he led two European Union funded "Alfa" projects for the cooperative research between several Latin American and European teams. He was one of the leaders for the IEEE International Caribbean Conference on Circuits, Devices and Systems (ICCDCS), and actively participated in the organization of the conference.

But above all, he was an extremely kind and pleasant person, friend and colleague. We will remember him with fond memories. Our community will miss him a lot. He is survived by his wife, his son and his grandson."

Fernando Guarin
IEEE Fellow
EDS President Elect 2016–2017

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

New EDS Field of Interest Approved by the EDS BOG
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.