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Newsletter

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Technical Briefs

ESD During Times of Change

Charvaka Duvvury, *ESD Technical Consultant and*
Harald Gossner, *Intel Mobile Communications*

The electrostatic discharge (ESD) threat is a perennial issue dating back to the beginning of the semiconductor technology development [1]. No one is quite certain when it was first observed and recognized as a real threat to the electronics industry but it has not received clear focus until the late 1970s when the first ESD symposium was held. It was during this time that both control measures were implemented in areas where ICs are handled (ESD protected areas), and ESD protection structures were added to the IO circuitry. As industry experts have realized that charges on humans is a major source of damage the commonly known Human Body Model (HBM) test was developed. Similarly discharge from packaged ICs touching grounded metal surfaces led to the introduction of Charge Device Model (CDM). Applying these test models typical failures found during handling of semiconductors can be reproduced (Figure 1). They are distinctly different to extended fails when an electronic system is hit by a massive electrical overstress or ESD discharge (Figure 1). For many years it was believed that IC design protection to 2000 V HBM and 500 V CDM should be absolutely required for safe production and handling. However, this scenario started changing due to aggressive device scaling effects starting during the early 1980s and the demand for higher speed

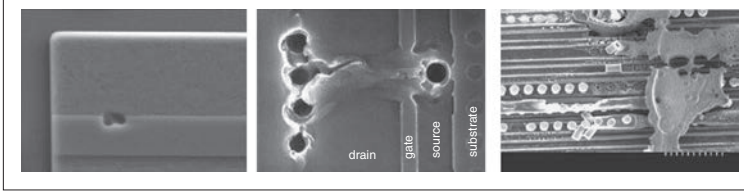

Fig. 1. IC damages due to ESD: CDM type (left), HBM type (middle), system level ESD (right).

(continued on page 3)

Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at radhakrishnan@ieee.org

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Newsletter Deadlines

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ESD During Times of Change

(continued from page 1)

circuits starting from late 1990s. As a result of Moore's Law, all of these technology developments continued to make a severe impact on ESD design which is now tending towards a *paradigm shift* to consider more practical ESD levels to accommodate circuit speed, performance, and reduced time to market of products.

From a device point of view it is well known that ESD robustness is gauged by the intrinsic second breakdown current level of a MOS device under parasitic bipolar *npn* breakdown as shown in the inset of Figure 2. Hole current due to drain avalanche gives rise to ISUB and IB, and the *npn* turns on when the local V_B' reaches 0.7 V. During this bipolar conduction J.E heating at the drain junction causes failure in the ESD time domain as measured by power dissipation at the Vt2, It2 point. The It2 measured as failure current per unit width with gate-sub grounded is FoM used for assessing the device technology impact.

The device scaling impact on It2 is indicated in Figure 3 where the different process technology features for IC production are indicated as markers. The early device scaling technology parameters of LDD and silicide resulted in the most severe impact on ESD which resulted in design challenges to meet 2 kV HBM. At the next level, thinner metal leads and reduced gate oxide thickness created more severe challenges for 500V CDM protection design. As technology advances continued, the High-k Dielectrics, FinFETs, and SOI all show negative impact on ESD design capability at the device level, while strain engineering has provided a slight increase in ESD design margin. Bulk FinFET is relatively more suitable than SOI FinFET for ESD (See Figure 4) [2]. A further degradation of ESD design margin

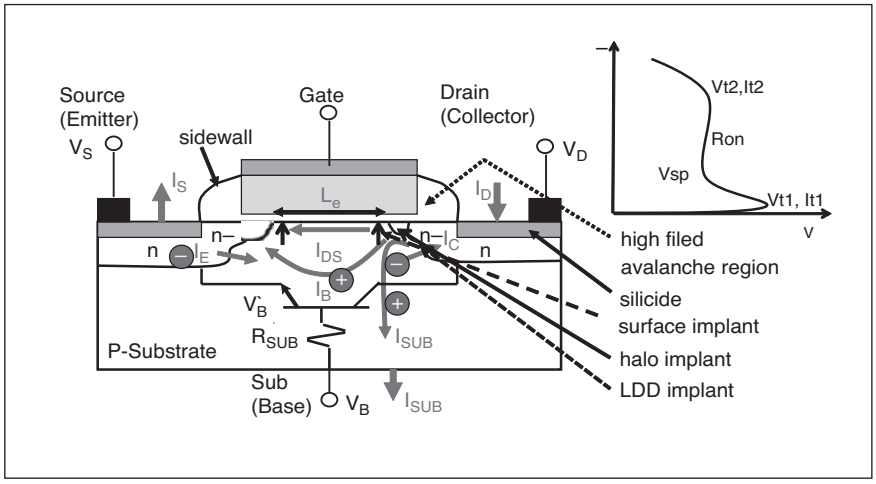

Fig. 2. NMOS device under high field bipolar breakdown.

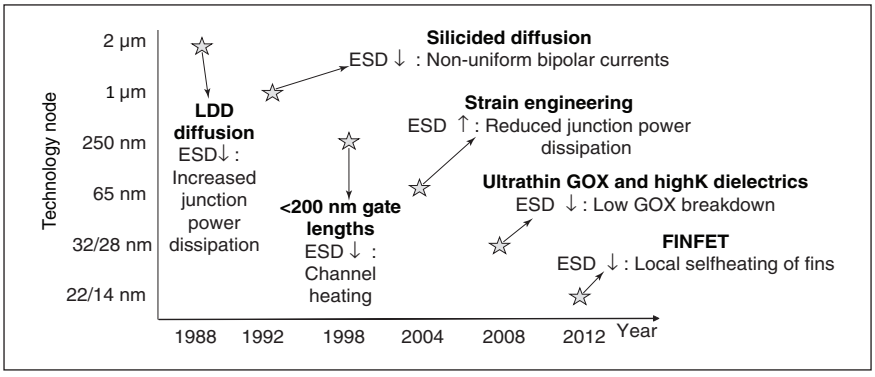

Fig. 3. Device scaling and technology effects on ESD robustness.

occurs due to the shrinking of metal interconnect width and thickness in the sub 22 nm technologies.

The full picture of ESD cannot be obtained without considering the advanced circuit designs that use the attractive features of device scaling. The impact from IC chip developments is shown in Table I. The demand for higher speed circuits with dense memories have led to both high speed serial link (HSS) IOs and the utilization of larger pin count IC packages. The combined effects of thinner gate oxides with the corresponding lower breakdown voltages, less tolerance to ESD loading capacitance to maintain higher data rates, and increased ESD discharge currents from the larger IC packages, have all led to reduced ESD protection levels. As an example the composite impact on HBM ESD for 20 Gb/Sec is illustrated in Figure 5 [3]. The design window closes with reduced oxide thickness (BVox) and thinner metal interconnects (JMESD). In a similar manner CDM is also severely impacted forcing <125 V protection below the 14 nm node due to the additional effect from larger microprocessor IC package sizes with relatively higher discharge currents.

To accommodate both advanced device technologies and high performance circuit demands, practical

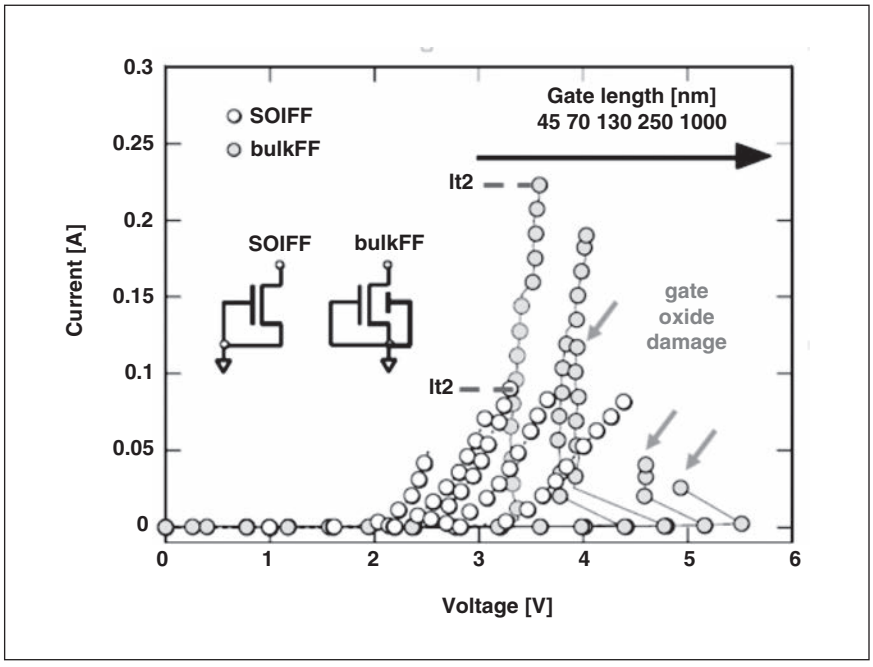

Fig. 4. Relatively higher It2 performance for Bulk FinFET vs SOI FinFET [2].

Design Feature	Memory Sizes	ESD Design Constraints	Impact on ESD Levels
DRAMs SRAMs EPROMs	1K to 1Meg	Mild	2kV HBM 500V CDM
Microprocessors <5 Gb/s	> 1Meg	Moderate	1kV HBM 250V CDM
High Speed Microprocessors > 20 Gb/S	> 4 Meg	Severe	500V HBM 125V CDM
Analog Designs SoC HV Analog	N/A	Mild/Moderate	2kV HBM 500V CDM
RF	N/A	Severe	500V HBM 300V CDM
SiGe	N/A	None	2kV HBM 500V CDM
GaN	N/A	Severe	300V HBM 125V CDM
3-D ICs (only at micro-bumps & internal interfaces)	N/A	Very Severe	100V HBM 50V CDM

Moore's Law

Emerging Tech.

Table I. IC Circuit Design Effects.

ESD levels necessary for safe production had to be reexamined. With this mission the Industry Council on ESD Target Levels was founded in 2006 and eventually established that 500 V HBM and 250 V CDM are just as safe allowing better opportunities for qualification of high end products which is discussed in depth in JEDEC approved documents [4] [5].

The most problematic issues for ESD will begin to surface with some of the emerging technologies such as GaN and 3D ICs. Similar to GaAs, GaN does not have intrinsic bipolar device advantage and the ESD protection can be severely reduced to 300–400 V HBM range [6]. For 3D IC interfaces, area constraints and signal transition at high speeds of the die–to-die interfaces would not allow much ESD protection to be implemented making it even more challenging in future [7]. While the exposure to ESD events during manufacturing is believed to be low, a statistical evaluation of ESD sensitivity of 3D IC manufacturing is yet to be clearly established.

ICs with advanced devices are becoming more sensitive to ESD but they can still be safely manufactured with improved ESD control methods in the factory [8]. This ability goes in parallel with IC customers accepting the new ESD target levels as mentioned above. Recently the focus is shifting from impact of on-chip protection on ESD to discharges on systems that use these advanced devices. In mobile phone systems and laptop computers, although the ICs are embedded, critical external interfaces exist like USB 3.0 and HDMI. In the end user system, the ESD threat is coming from external sources outside the ESD control areas and is much harsher (nearly at 8kV levels with much higher current levels than HBM or CDM). This scenario is shown in Figure 6. At 28nm technologies with data rates going towards 5GB/s for both the USB3 and HDMI the challenge to meet ESD-safe consumer products becomes even more severe. This calls for "co-design" efforts for protecting the systems with advanced technology products by using effective simulation approaches. These issues are given in the Industry Council JEDEC documents [9] [10]. The details of a new system efficient ESD design (SEED) for system ESD protection is introduced in an upcoming book [11].

As electronic industry moves ahead to more challenging technologies and systems, ESD circuit design, testing and ESD control will

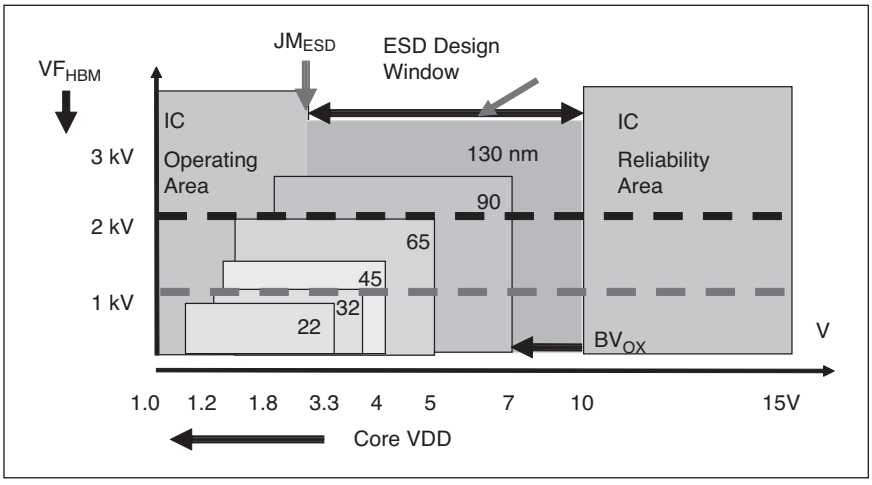

Fig. 5. Reduced ESD Design Window with advanced devices.

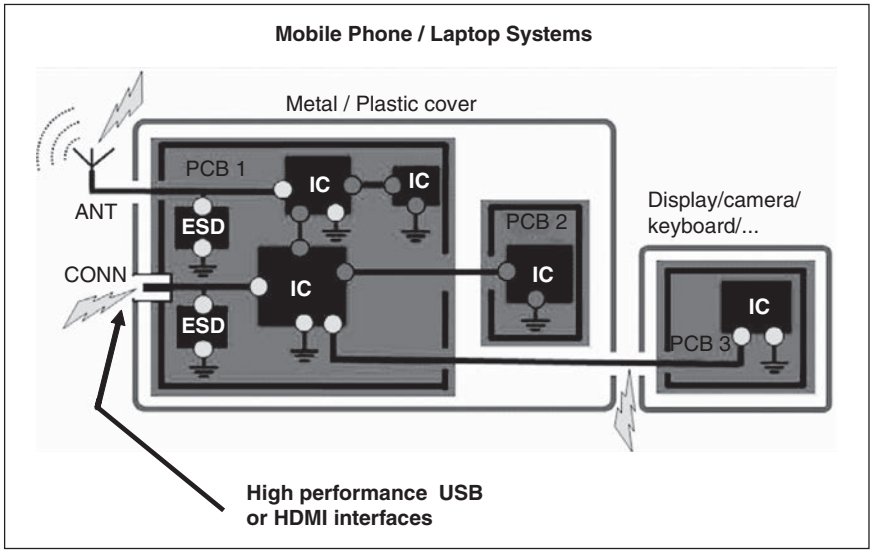

Fig. 6. A consumer system exposed to system ESD at external ports.

stay to be a vivid field of research and development. This should serve as a good outlook and as prospective enticement for engineers and researchers who would want to become involved in this crucial area of electronics reliability.

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Charvaka Duvvury *was a Texas Instruments fellow where he worked in the silicon technology development group. He is currently working as a technical consultant on ESD design methods and ESD qualification support. He has published over 150 papers in technical journals and conferences and holds 75 patents. He has co-authored books on ESD design, hot carriers, and modeling of electrical overstress. He is a recipient of the Outstanding Contributions award from the EOS/ESD Symposium (1990), Outstanding Mentor award twice from the SRC (1994 and 2012), and numerous best paper and best presentation awards from the EOS/ESD Symposium. He received the IEEE Electron Devices Society Education award in 2013. He was a contributing editor for the IEEE Transactions on Device and Materials Reliability (TDMR) from 2001 to 2011. Charvaka is an IEEE Fellow. He has been a member of the EOS/ESD Association board of directors since 1997, promoting university education and research in ESD. He is a co-founder and co-chair of the Industry Council on ESD Target Levels.*

Harald Gossner *is a Senior Principal Engineer at Intel. He received his degree in physics (Dipl. Phys.) from the Ludwig-Maximilians-University, Munich in 1990 and his Ph. D. in electrical engineering from the Universität der Bundeswehr, Munich in 1995. For 15 years he has worked on the development of ESD protection concepts with Siemens and Infineon Technologies. In 2010 he joined Intel Mobile Communications overseeing the development of robust mobile systems. Harald Gossner has authored and co-authored more than 100 technical papers and two books in the field of ESD and device physics, and he also holds 50 patents. He received the best paper award of EOSESD Symposium in 2005 and in 2012. He is regularly lecturing ESD tutorials at IEEE conferences and is member of the board of directors of ESD Association. In 2006 he became cofounder and co-chair of the Industry Council on ESD Target Levels.*

EDS Partners with SRC and SEMI at SEMICON WEST – "The Path to Future Interconnects"

Jonathan Candelaria, Semiconductor Research Corporation

The rate of improvement in high performance computing has slowed dramatically. A large part of this has been caused by the energy constraints coming from moving data across interconnect networks. The architecture that has driven the exponential growth in computing for over 50 years has led us to this point by requiring data to be transported between the processing and memory parts of the system, and more recently also between multiple processing cores in a chip.

Evolutionary approaches to address this challenge are increasingly ineffective, and breakthroughs can happen now only with a system-level approach, and co-optimization from novel materials and processes, through emerging device designs and circuits, to revolutionary system architectures. More broadly, effective and efficient interconnectivity is essential for enabling every electronic system, from internet data centers and business servers to portable and wearable electronics, and to the individual sensor nodes that interface with the physical world in IoT environments.

Recognizing these broad set of critical challenges, the IEEE EDS partnered with the Semiconductor Research Corporation (SRC) and the Semiconductor Equipment and Materials International (SEMI) to organize and host a day-long workshop on "The Path to Future Interconnects" at SEMICON West, held at the Moscone Center in San Francisco, July 16, 2015.

The whole day program had 8 speakers represented by semiconductor industry leaders Applied Materials, Lam Research, IMEC, and GLOBALFOUNDRIES, as well as leading academic institutions Georgia Tech, Columbia University, and UC-Berkeley. Because of the breath of topics to be covered, two half-sessions were conducted, each with a speakers' panel that followed their presentations (http://www.semiconwest.org/node/13836).

In both half-sessions, presentations on the impact of interconnect choices on circuit performance and likewise the constraints and requirements placed on interconnect technology by circuit and system needs set the stage for the following talks.

In the first half-session discussed the challenges for interconnect technology up to the end of the CMOS roadmap, and a few of the emerging materials and processing alternatives to address them. The speakers Mehul Naik of Applied Materials and Larry Zhao of Lam research discussed the challenges, whereas the circuit impact of interconnects was described by Azad Naeemi of Georgia Tech. Rama Alapati of GLOBALFOUNDRIES presented state of 3DIC technology

In the second half-session, possible directions beyond the roadmap were discussed, such as spin-based technology and nanophotonic solutions. Then the interconnectivity requirements and solution paths for newly emerging applications such as flexible and stretchable electronics for wearable applications were described and demonstrated. Karen Bergman of Columbia University showed the photonic interconnection networks for high performance computing. Interconnects for flexible/stretchable circuits was explained by Jan Vanfleteren of IMEC. The talk that wrapped up the workshop was a thought-provoking presentation by Jan Rabaey of UC Berkeley on brain-inspired connectivity architectures and technology that have been gaining traction recently and offer real hope for a long and bright future for semiconductor technology and the electronics industry as a whole.

Upcoming Technical Meetings

2015 IEEE International Electron Devices Meeting (IEDM)

(The Latest Technology Developments in Micro/Nanoelectronics)

Gary Dagastine and Chris Burke

When the world's leading scientists and engineers in micro/nanoelectronics convene in Washington, DC this December for the 61st annual IEEE International Electron Devices Meeting (IEDM), the subjects under discussion will encompass a range of topics critical to the continuing progress of the industry:

- how to make transistors that are vanishingly small
- a growing emphasis on low-power devices for mobile & Internet of Things (IoT)
- alternatives to silicon transistors
- 3D IC technology

A broad range of papers that address some of the fastest-growing specialized areas in micro/nanoelectronics, including silicon photonics, physically flexible circuits and brain-inspired computing will be discussed.

The 2015 IEDM will take place at the Washington D.C. Hilton Hotel from December 7–9, 2015, preceded by day-long short courses on Sunday, December 6th and a program of 90-minute tutorials on Saturday, December 5th. In addition to a technical program of some 220 papers, a rich offering of other events will take place during the meeting, including evening panels, special focus sessions, IEEE awards and an entrepreneurial luncheon sponsored by IEDM and IEEE Women in Engineering.

Back by popular demand for the third year, the 2015 IEDM will feature a slate of designated focus sessions on topics of special interest. This year's topics are:

- Neural-Inspired Architectures: From Ultra-Low Power Devices To Applications
- 2D Layered Materials And Applications
- Power Devices And Their Reliability On Non-Native Substrates
- Flexible Hybrid Electronics
- Silicon-Based Nano-Devices For Detection Of Biomolecules And Cell Functions

"From its inaugural meeting until today, the IEDM conference has been the place where breakthroughs that drive the electronics industry forward are unveiled," said Mariko Takayanagi, IEDM 2015 Publicity Chair. "For example, at the IEDM in 1975 Intel's Gordon Moore gave a talk that refined his earlier prediction of transistor scaling into what has since become known as Moore's Law. That tradition of attracting the best speakers and a large, diverse audience from around the world continues, with a focus this year on devices intended to support the Internet of Things and other emerging areas of importance that depend upon advances in semiconductor technology." Here are some of the noteworthy events that will take place at this year's IEDM:

90-Minute Tutorials on Saturday, December 5th

A program of 90-minute tutorial sessions on emerging topics will be presented by experts in the fields. They are meant to bridge the gap between textbook-level knowledge and leading-edge current research. The tutorials will be presented in parallel in two time slots.

- *Electronic Control Systems for Quantum Computation*, by David DiVincenzo, Aachen University
- *Advanced Device Concepts for 7 nm Node and Beyond*, by Scott Thompson, University of Florida
- *Thin Film Transistors for Displays and More,* by Tom Jackson, Pennsylvania State University
- *Nanoscale III-V Compound Semiconductor MOSFETs for Logic*, by Luca Selmi, University of Udine
- *RF and Analog Device Technologies*, by Anthony Chou, GLOBALFOUNDRIES
- *Implantable Sensors and Electronics for Brain Interfaces*, by Euisik Yoon, University of Michigan

Short Courses on Sunday, December 6th

The IEDM will host two Sunday short courses, giving attendees the opportunity to learn about important areas and developments, and to benefit from direct contact with expert lecturers. Advance registration is required. This year's courses are:

- *Emerging CMOS Technology at 5 nm and Beyond,* organized by Yuan Taur, UC San Diego
- *Memory Technologies for Future Systems,* organized by Dirk Wouters, Aachen University

Plenary Presentations – Monday, December 7th

IEDM 2015 will open on Monday, December 7th at 9 a.m. with three plenary talks:

- *Moore's Law: From 50 to Retirement,* by Greg Yeric, ARM
- *Silicon for Prevention, Cure and Care: A Technology Toolbox of Wearables at the Dawn of a New Health System*, by Chris Van Hoof, Imec
- *Atomic-Scale Electronics for Quantum Computing,* by Michelle Simmons, University of New South Wales

Some of the key papers/presentations include:

- *New NAND Architecture* by Macronix;
- *InGaAs Nanowire FETs on Silicon* by IMEC;
- *High-Frequency, Low-Leakage IGZO Transistors for Internet of Things* by Semicon Energy Laboratory;
- *Monolithic 3D Chip* by National Nano Device Laboratories;
- *Better GaN HEMTs for High-Power Amplifiers* by Fujitsu/ Tokyo Institute of Technology;
- *Artificial Synapses for Learning* by IBM

Evening Panel Session – Tuesday, December 8th

The IEDM offers attendees two evening sessions featuring panels of experts. Audience participation is encouraged to foster an open and vigorous exchange of ideas.

- *Is There a Potential for a Revolution in On-Chip Interconnect?* moderated by Paul Franzon, North Carolina State University
- *Emerging Devices: Do They Address the Real Issues?* moderated by Heike Riel, IBM

Entrepreneurs Lunch – Wednesday, December 9th

Jointly sponsored by IEDM and IEEE Women in Engineering, the Entrepreneurs Lunch at IEDM is back for a fourth year. The speaker will be Abbie Gregg, President of AGI Abbie Gregg, Inc. Abbie has more than 25 years of experience as an engineering consultant, and 30 years of experience in cleanrooms, labs and imaging spaces. She specializes in process engineering and analysis, facility layout and design, quality assurance, equipment selection and qualification. AGI Abbie Gregg, Inc. was founded in 1985 and has extensive experience in nanotechnology, biotechnology, photovoltaic, wafer fab, assembly, multichip module, etc., and has more than 800 projects on five continents.

Further information about IEDM:

For registration and other information, visit the IEDM 2015 home page www.ieee-iedm.org, or contact:

Phyllis Mahoney, Conference Manager, Widerkehr & Associates, 19803 Laurel Valley Place,

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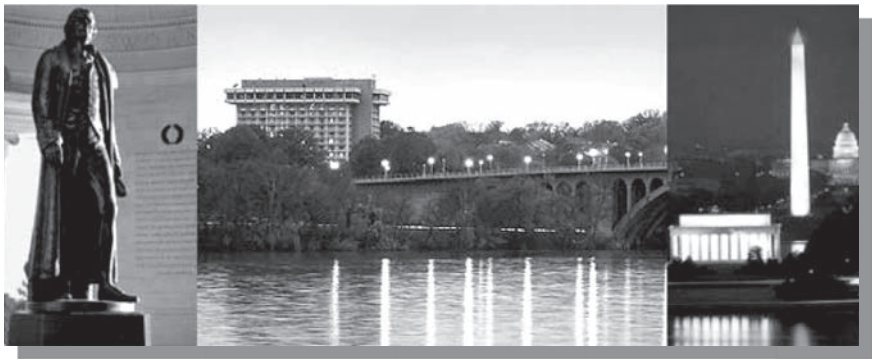
2015 IEEE Semiconductor Interfaces Specialists Conference (SISC)

The 46th IEEE Semiconductor Interface Specialists Conference (SISC) will be held at Key Bridge Marriot Hotel in Arlington, Virginia, on **December 2–5, 2015**, immediately prior to the IEEE International Electron Devices Meeting (IEDM) in Washington, DC. An evening Tutorial session, free to all registered SISC attendees, will be held on December 2nd.



Washington DC, attractions are within easy reach from Key Bridge Marriot Hotel

The SISC is a workshop-style conference that provides a unique forum for device engineers, materials scientists, and solid-state physicists, to openly discuss issues of common interest. Principal topics are semiconductor/insulator interfaces, the physics of insulating thin films and the interaction among materials science, device physics, and state-of-the-art technology. Emphasis is placed on current and future nanoscale device architectures, and how interfaces between dissimilar materials and ultra-thin films affect device operation where theory, modeling/ simulation, and characterization

results are used to help understand the impact on device performance and reliability. The conference alternates between the East and West Coasts, and meets just before the IEDM to encourage the participation of IEDM attendees. SISC is sponsored by the IEEE Electron Devices Society.

An important goal of the conference is to provide an environment that encourages interplay between scientific and technological issues. Oral sessions of invited and contributed talks, as well as a lively poster session, are designed to encourage discussion. Conference participants have numerous opportunities for social gatherings with renowned scientists and engineers. They also enjoy Washington, DC attractions such as the National Mall with the Lincoln Memorial, the National Air and Space Museum, the National Gallery of Art, the White House, the US Capitol, and the Library of Congress.

Conference focus

The program includes about 70 presentations from all areas of MOS science and technology. The topics evolve with the state-of-the-art, and include:

- **SiO_2** and **high-k dielectrics** on Si and their interfaces
- **Insulators on high-mobility and alternative substrates** (SiGe, Ge, III-V, SiC, etc.)
- MOS gate stacks with **metal gate electrodes**
- Stacked dielectrics for **non-volatile memory**
- **Oxide and interface structure**, chemistry, defects, passivation: theory and experiment
- **Electrical characterization, performance and reliability** of MOS-based devices
- **Surface cleaning technology** and impact on dielectrics and interfaces
- Dielectrics on **nanowires/tubes, graphene**
- **Oxide electronics** and **multiferroics**
- **Interfaces in photovoltaics,** e.g. Si passivation
- **2D materials and devices** and their interfaces

Invited presentations

This year's invited presentations will include:

- **Dr. Mikhail Baklanov**, imec, Belgium
  Ultralow-k insulating materials for 10-nm technology node and beyond
- **Prof. Massimo Fischetti**, UT Dallas, USA
  Physics of electronic transport in low-dimensionality materials for future FETs
- **Prof. Andrew Kummel**, UCSD, USA
  Monolayer Organic Films for Nucleation of ALD on Single Layer Graphene and TMD surfaces
- **Prof. Masaaki Kuzuhara**, Fukui University, Japan
  GaN-based HEMTs for High-voltage and Low-loss Power Applications
- **Prof. Blanka Magyari-Kope**, Stanford University, USA
  Microscopic Aspects of Conductive Filaments Evolution in Metal Oxide RRAM devices
- **Dr. Alessandro Molle**, MDM Laboratory, Agrate Brianza, Italy
  Silicon at the two-dimensional limit: the debut of the silicene transistor
- **Prof. Akira Toriumi**, University of Tokyo, Japan
  Materials and Process Controls for Scaled Germanium Gate Stacks
- **Prof. Wenjuan Zhu**, University of Illinois, Urbana-Champaign, USA
  Two-dimensional Layered Materials and Nano-scale Devices

Wednesday evening Tutorial – free to all registered SISC attendees

- **Dr. Iuliana Radu,** imec, Belgium
  Spin logic options for Beyond or Along CMOS

Unique poster program

A unique feature of SISC is the attention paid to the poster presentations. Each author of a poster presentation has the opportunity to introduce their work orally, using two visuals, to the entire SISC audience during special poster introduction sessions. The posters are then presented during a separate poster reception on Thursday evening, the second poster session on Friday afternoon followed by the conference banquet.

Best Student presentation award

SISC is a popular conference with students, who can get immediate and candid feedback on their latest results from the experts in the field. In addition to a strongly reduced registration fee for students, a Best Student Presentation award is given every year in memory of E.H. Nicollian, a pioneer in the exploration of the metal-oxide-semiconductor system who had a strong presence within the SISC.

Accompanying program

The scientific content of the conference is complemented by informal events designed to encourage lively discussion and debate. A hospitality suite with complimentary drinks is available to attendees to continue their discussions on every evening of the conference. On Friday evening the conference hosts a banquet and awards ceremony, complete with the now-famous (and always riotous) limerick contest. The limericks never fail to give the conference presentations, people and events an entirely new perspective.

SISC is always a rewarding experience for specialists, students, as well as newcomers to the field. For more information about the conference, to consult its program and to register, please visit **http://www.ieeesisc.org**. We look forward to seeing you at SISC 2015!

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Society News

Message from EDS President-Elect

Samar Saha
EDS President-Elect

It is worth reiterating that *the IEEE Electron Devices Society (EDS) is a volunteer-driven volunteer-led technology-centric organization*. The volunteer engagement in the *state-of-the-affairs* of the society is crucial to sustain and broaden EDS's field-of-interest (FOI) in the new frontiers of device physics and process technology. In EDS, it is encouraging to the see active participation of its volunteers in the society affairs leading to the positive changes for the benefit of the society.

The participation of EDS volunteers at the mid-year EDS Board of Governors (BoG) meeting series on May 30–June 1, 2015, at Marina Mandarin Hotel, Singapore, was overwhelming. This Region 10 venue for EDS BoG meeting series offered opportunities for EDS BoG members to hear and network with the members of the Region in the Chapter and BoG meetings as well as during Open Forum discussions. I envision a similar EDS member involvement in the 2016 mid-year BoG meeting series at the beautiful city of Grenoble, French.

In the recent years, the active involvement of EDS volunteers is leading the improvements in societal governance including written documents of standing and technical committee charters, updated constitution & by-laws, selection of Editor-In-Chief (EIC) of EDS publications, and so on. One of the immediate outcomes of these changes is the open EIC selection process for the *IEEE Transactions on Electron Devices* and *IEEE Electron Device Letters* by the Publications and Products committee. The changes will continue through further discussions among BoG and Forum members to have a clear consensus among all EDS members to create permanent documents for all society practices and governance.

Apart from participating in EDS's technical and standing committees and chapters, I strongly encourage each member to participate in EDS governance as elected member and annual election process. The society needs fresh beautiful minds as new elected members to run its technical activities and elevate EDS to a new level of technical excellence! I invite each member to participate in the 2015 *General Election* process to elect your representative who can contribute to the society with new ideas and convictions.

It is crucial for EDS to engage students and young professionals in EDS activities for continued success and growth of the society. In order to encourage students and young professionals, the society has several awards program such as *Masters and Ph.D. Student Fellowships* and *Early Career Award.* I encourage EDS members in academia and industry to nominate students and young professionals for the respective award.

In summary, it is encouraging to see volunteer engagement in EDS *state-of-the-affairs* to ensure transparencies in society governance. It is important that each and every EDS member from all IEEE regions gets involve in the key areas of EDS endeavors to elevate the society and its FOI to a new height.

See you all at the December 2015 BoG meeting series in Washington, DC.

Samar Saha
President-Elect
Prospicient Devices
Milpitas, CA, USA

Message from Newsletter Editor-in-Chief

M K Radhakrishnan
Editor-in-Chief,
EDS Newsletter

Dear Readers,

As the Newsletter is now available at the finger tips through a mobile compatible Flipbook version which is accessible to everyone, the publication is exposed to the whole world and our reader base increases. As such, we are introducing various new columns as well. However, a number of readers have commented that the hard copy version is more valuable and enticing for reading and reference. With the regular featuring of technical articles on various aspects related to device technology appealing to readers at all levels, it is our aim to keep continuing the present structure of the publication unabated.

The main technical article in this issue deals with one of the major threats device technology faces from the very early days and still continuing as we go through the nano scale to atomic dimension. How the ElectroStatic Discharge (ESD) poses detrimental effects to Electron Devices and Systems (EDS) is strikingly narrated in the "ESD during Times of Change" which is the second article in device reliability trends series to appear in the Newsletter.

Reports and highlights of three EDS Technical Committees (TC) and their deliberations are featured in this issue. TCs on Semiconductor Manufacturing, Power Devices, and VLSI Technology and Circuits discuss the latest trends and the mode by which the committees plan to enrich the areas through various types of activities and participation in conferences, publication, etc.

We are introducing a new feature to cover EDS Chapters' reflections in the community in the Chapter News section. The first article under this category describes how an EDS chapter could contribute in a subtle way as stimulus in the technology growth in a region. In future, we will try to bring articles highlighting such Chapter's contributions to the community.

The feature on Reflections from Young Professionals introduces an interview with aYP from the industry very close to EDS in many ways. We are trying to cover this feature with a different style through a mix of interviews and thoughts from young and aspiring professionals both in academia, research and industry.

I would like remind all readers that it is a collective effort from a team to make this volume as such in front of you. Unless we hear your views, both constructive and critical, we may not be able to further improve. I urge every reader to write your opinion to either edsnewsletter@ieee.org or to me radhakrishnan@ieee.org

M K Radhakrishnan
Editor-in-Chief, EDS Newsletter
radhakrishnan@ieee.org

Message from EDS VP Membership and Services

Mikael Östling
EDS Vice-President of Membership & Services

As for all professional societies our primary concerns are the member benefits. What's encouraging is that EDS is one of the IEEE's largest societies and the good news is that we have been able to keep our member count constant over the past few years when many other societies see marked decline in membership. EDS has a steady member count of just over 10000 members. This is a fairly good membership level but we can do better. Very positive is that our student member numbers are increasing as well as the affiliates count.

Over the past few years we have launched several activities that provide added values for our members. In 2011, the EDS webinar series came on line and delivers live lectures with luminaries from the field of electron device engineering... streaming right into your desktop! Just recently we have presented two very exiting webinar events;

"Terahertz Electronics for Sensing Applications" presented by Prof. Michael Shur, Rensselaer Polytechnic Institute, Monday, at the end of July and

"Engineering a Sustainable Society with Power Semiconductor Devices," presented by Jayant Baliga, North Carolina University at the end of August.

Later webinar events in this series will tentatively treat plagiarism/authorship/copied work/research fraud, Graphene and 2D Materials, 3D Integration and ESD, and Bio integrated electronics

More benefits for our members that should be mentioned is that we have partnered with our colleagues at Semiconductor Equipment and Materials International (SEMI) in presenting two exciting programs at the upcoming SEMICON West 2015. Our thanks to long-time EDS volunteer, Jon Candelaria, for leading this effort on behalf of the society.

The featured programs focused on: *"The Path to Future Interconnects."* In this seminar Industry experts discussed the challenges in materials and processing of interconnects, examine the impact on circuit and system requirements and provide an outlook on the road ahead. Topics will include interconnect performance and yield challenges for 7nm and beyond, challenges and solutions for Cu and non-Cu, and interconnects for *"Beyond CMOS"* devices and circuits, including flexible, printed electronics. The second seminar focused on *"Packaging: Digital Health and Semiconductor Technology."* Hopefully we can continue this partnership for the future.

Moreover the EDS membership allows access to the archive webinar seminars where we recently had several hot technology topics such as *"CMOS device scaling"* by Prof. Yuan Taur, *"FINFETs"* by Prof. Chenming Hu, *"Circuits on Cellulose"* by Prof. Andrew Steckl. In addition, a whole range of career advice seminars can also be found in the archive. Just to a mention a few recent ones: *"Optimize Your Career through Graduate School"* by Prof. Mark Law, *"Working Successfully in the Semiconductor Industry"* by Dr. Doug Verret, and *"Reflections on the Gentle Art of Teaching and Mentoring"* by Prof. John Cressler.

We recently held several promotional campaigns such as the EDS Membership Fee Subsidy Program, which is A One Time Offer per Member – Free IEEE and EDS Memberships for new or renewing members of chapters located in developing nations. That was successful and resulted in a total of 120 new members for 2014 involving 13 chapters and 175 members. Last November, an EDS Webinar Recruitment e-mail promotion was run with complimentary EDS membership to non-IEEE member attendees of EDS webinars. We continue to run the Membership Campaign and Exhibits at premier IEEE EDS sponsored conferences.

During the membership and services committee meeting in Singapore in May this year we had an interesting discussion with ideas on how to increase the member benefits. Some of the conclusions were to continue to focus on young professionals and affiliate members, focus on on-line membership and improve the way we promote EDS at events such as Distinguished Lectures (DL). We will also continue the focus on webinar offerings.

Please remember to promote the EDS anniversary book "Guide to State-of-the-Art Electron Devices," edited by Professor Joachim N. Burghartz, with contributions by more than 50 EDS members. This book recently won the PROSE award and marks the 60th anniversary of the IRE electron devices committee and the 35th anniversary of the IEEE Electron Devices Society. I hope that all university supervisors promote their students to enroll as student members in EDS.

The success of EDS depends mostly on you, our valuable members, your continued input, ideas and voluntary work. Please send your comments to us. You are always invited to share your ideas. You can preferably do this by e-mail to Joyce Lombardini, who is the EDS Membership Administrator, e-mail: j.lombardini@ieee.org

Mikael Östling
EDS Vice-President of Membership & Services
KTH, Royal Institute of Technology
Sweden

Technical Committee Reports

EDS Power Devices and ICs Technical Committee Report

Don Disney
EDS Power Devices and ICs Technical Committee Chair

The power devices and ICs Technical Committee (TC) of the EDS has a charter to monitor the status of EDS meetings, education programs and activities, publications and awards in areas of power semiconductor devices and ICs. In the past couple of years, committee membership was refreshed and expanded to include more geographical diversity. We now have 13 members representing 8 countries. We meet annually during IEDM and also at the ISPSD, which is EDS-sponsored and is the premier conference in this field.

In 2014, our TC conducted an internal survey to assess the state of the committee and prioritize activities. The members unanimously said that EDS conferences and publications are already the most important and influential in our field. We decided to focus our efforts for 2015 in three areas:

- Education. Develop a series webinars to introduce students and new engineers to the field of power devices.
- Publication: Organize a special TED edition on state-of-the-art power devices and ICs.

- Conferences: Develop a list of power device conferences that are not currently affiliated with EDS and assess whether we should engage with them.
- Standards: Initiate or participate in an activity to develop reliability standards for wide bandgap power devices

So far, we have identified three speakers to kick-off our webinar series in 2015, starting with a webinar on August 26th by Prof. B. Jayant Baliga on Engineering a Sustainable Society with Power Semiconductor Devices. We plan to continue this series in 2016 to build a webinar archive covering all key aspects of the field.

We are presently working with the editor to arrange a special edition of TED that covers the state-of-the-art in power devices and ICs. There hasn't been such an edition in more than 20 years, so we are expecting to solicit many good contributions and high reader interest.

More information on this EDS TC can be found at: http://eds.ieee.org/technical-committees/eds-power-devices-a-ics-technical-committee.html.

Don Disney
EDS Power Devices and ICs
Technical Committee Chair
GlobalFoundries, USA

EDS Semiconductor Manufacturing Committee Report

Rajendra Singh
Chair, EDS
Semiconductor
Manufacturing
Committee

Since the invention of integrated circuits (ICs) in 1958, semiconductor manufacturing, popularly known as "chip manufacturing," has played a vital role in bringing forth a fundamental revolution in virtually every aspect of human life. The phenomenal growth of communication industry in general and the telecom industry specifically has been possible due to ultra-large-scale chip manufacturing based on low-cost and abundant silicon. According to Intel prediction, since the discovery of transistor in 1947, 1,200 quintillion (1.2×10^{21}) transistors will be manufactured by the end of year 2015. Today, the most advanced semiconductor manufacturing is based on 14 nm feature size circuits and employs 3-D manufacturing compared to planar circuit manufacturing in the beginning. More than 90 % of $1.5 Trillion global electronics business is based on silicon CMOS based semiconductor products. Lithography, process variability, and new materials have been key challenges in reducing feature size and advanced process control has played a central role in the design for manufacturing. (DFM).

The success of semiconductor manufacturing has been possible largely due to reduction of feature size, larger wafer size, reduction of defect density, providing more functionality at lower cost with the net result of semiconductor products with higher speed, lower size and lower cost. Providing process tools with lower foot print and lower cost of ownership and solving process integration problems are some of the innovation that are provided by tool manufacturers. Functional devices have been demonstrated in the range of 5–10 nm. Lithography has played more important role than any other processing step. Currently, 193 nm light source is used in *multi*-patterning *lithography of sub 14 nm semiconductor manufacturing. The additional cost of using multi-patterning is one of the barriers in semiconductor manufacturing in sub-10 nm range.* The *extreme ultraviolet* (EUV) light used in *EUV lithography* has a wavelength of 13.5 nm. Lithography based on EUV has the potential of reducing patterning cost and can be an enabler of sub-10 nm manufacturing. It is worth mentioning here that the large investment of human and capital resources in the last 15-20 years in the so called "bottom-up", "nanotechnology" manufacturing had no contributions to semiconductor manufacturing.

The complexity of semiconductor manufacturing offers more opportunity to others to help the manufacturing technologies. Efforts that lie in EDA, process control, failure analysis, packaging and integration become ever more critical to decompose problems in a timely basis for solution. There is a range of art on what the state of the art in what process design and yield management is.

Other than the conventional growth areas of the semiconductor products (digital, analog, RF and mixed signal), new growth areas are emerging. One such area involves "internet of things" (IOT). It is estimated that by the year 2020, the number of connected things may reach 50 billion. The use of IOT in connecting people, process, data and things will create opportunities for new revenue streams, new options for competitive advantage, and new operating models to drive both efficiency and value, potentially driving massive gains in efficiency, business growth, and quality of life all over the world. From manufacturing point of view, various types of sensors will be integrated with silicon chips. The integration will come by the system on chip, system in packages and 3-D packaging routes. Both tool manufacturers and Fab owners have to find cost-effective ways to meet the demand of IOT based semiconductor products. The use of field programmable gate array (FPGA) architecture will solve

some problems of IOT based semiconductor products.

The power industry is providing another growth area for semiconductor manufacturing. As we are moving away from centralized power generation of the 20th century to clean distributed power generation in the 21st century (use of "microgrids" and "nanogrids" in digitally controlled electricity infrastructure), cyber security becomes very important for electricity infrastructure and electricity based surface and water transport sector. New computer chips will offer on-chip security features, such as secure storage, cryptographic accelerators, and tamper resistance mechanisms.

Innovations of all segments of semiconductor manufacturing are required to continue the semiconductor product cost reduction path of the last several decades. Fundamental research on new materials, their interfaces, new processes and new devices is certainly required if we are ever to achieve practical semiconductor products with sufficiently low power consumption for products manufactured with critical dimensions approaching 5 nm or less.

The 2015 EDS Semiconductor Manufacturing Committee members are from Applied Materials, ASML, Clemson University, Intel Corporation, LoPel Corporation, Qualcomm, RTI International, SUNY Polytechnic Institute, Tsinghua University, Toshiba Corporation, University of Colorado at Colorado Springs, and Xilinx. Contact details of committee members can be found at: http://eds.ieee.org/technical-committees/semiconductor-manufacturing.html

Three of the committee members (Rajendra Singh, Klaus Schuegraf and Alain Diebold), as well Luigi Colombo and Robert Doering of Texas Instruments were authors of the chapter "Semiconductor Manufacturing" of the EDS anniversary book *Guide to State-of-the-Art Electron Devices*, J. Burghartz, ed., Wiley-IEEE, 2013. Bo Lojek and Alain Diebold serve as members of the editorial board of *IEEE Transactions of Semiconductor Manufacturing* (TSM) in the area of Equipment and Process Technology and Metrology, respectively. Geoffrey Yeap was keynote speaker at IEDM 2013. Rajendra Singh and Hidetoshi Koike have served as Guest Editors of Special Sections of IEEE TSM. For a number of years Hidetoshi Koike was involved in the organization of the semiconductor manufacturing conference, ISSM.

Rajendra Singh
Chair, EDS Semiconductor Manufacturing Committee
Clemson University, USA

EDS VLSI Technology and Circuits Committee Report

On June 17, 2015, the EDS VLSI Technology and Circuits Committee met in Kyoto, Japan during the 2015 SYMPSOIUM ON VLSI TECHNOLOGY meeting, June 16–18. This committee has face to face meetings twice a year during the IEDM and VLSI Symposiums.

The objective of *the* VLSI Technology and Circuits Committee is to identify new and relevant areas of interest to the Electron Devices and Solid-State Circuits communities. Based on the nature of the areas, the committee recommends any or all of the following:

1) Initiate topical workshops of current interest (attached to existing conferences or incorporated in new ones)
2) Special issues for major publications (e.g., T-ED)
3) Panel session topics for major conferences
4) Special sessions for major conferences

Standing from left to right – Masaaki Niwa, Reza Arghavani, Hiroshi Iwai, Shuji Ikeda, Steve Chung, and Hitoshi Wakabayashi

The following topics were discussed during the June meeting:

1) We welcome four new committee members starting in January of 2015:
   a) **John Suehle,** NISTCEA LETI
   b) **Mansun Chan,** Hong Kong University
   c) **Monuko du Plessis,** University of Pretoria
   d) **Hitoshi Wakabayashi,** Tokyo Institute of Technology

The committee now has representatives from Asia, North/South America, Africa and Europe.

2) Roles and responsibilities of the following subcommittees were discussed:
   a) **Publication Chair:** Steve Chang
   b) **Conferences/Workshops Chair:** Kaz Ishimaru
   c) **Publicity Chair:** Seiichiro Kawamura
3) The proposal from last meeting to create a new EDS Asian Flagship Conference was discussed in more detail:
   a) Industry (manufacturing) and academic related papers
   b) Exhibition from equipment companies
   c) Emerging devices, Bio/Medical, and related topics
   d) Tutorials
   e) Location: Taiwan, China, Korea and Japan (First Round)

The following in general were agreed upon:

- Name of the conference: AEDM (Asian Electron Device Meeting)
- Focus: Device technology
- Type of conference: To include devices technology, Exhibition, Tutorials etc., but differentiated from existing conferences.
- Mission:
  - Create new field that IEDM does not cover.
    - Enhance industry papers
    - Educate engineers/students
    - Keep high quality of papers
- Location: Taiwan, China, Korea, Singapore and Japan (First Round Location in Japan in conjunction with Japan Applied Physics Society Conference)

Please contact Dr. Kaz Ishimaru (kazu.ishimaru@toshiba.co.jp), conferences/workshops subcommittee chair, or Dr. Shu Ikeda (shu.ikeda@tei-solutions.com), committee chair, for further information.

Reza Arghavani
EDS VLSI TC Committee Member
Lam Research Corporation
Fremont, CA, USA

Awards & Recognition

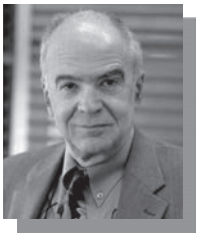
EDS Members Named Recipients of 2015 IEEE Medals

James Plummer of Stanford University has been named the recipient of the 2015 IEEE Founders Medal. His citation states, "*For leadership in the creation and support of innovative, interdisciplinary, and globally focused education and research programs.*"

James D. Plummer used his influence as the longest-serving dean of Stanford University's School of Engineering to support and lead major innovations that have changed the way engineering research and teaching is carried out, impacting industry and academia worldwide. Serving as dean from 1999 through 2014, Dr. Plummer led the efforts at Stanford to build major interdisciplinary centers to address challenges facing engineering in areas including energy, the environment, and biomedicine. The Precourt Institute for Energy was developed to focus on energy efficiency, distribution, and generation and features researchers spanning the spectrum of engineering disciplines. The Woods Institute for the Environment was created to address issues in environmental sustainability and features environmental engineering faculty. He also established Stanford's Bioengineering Department, jointly housed in the School of Engineering and the School of Medicine, to apply engineering principles to medical problems and biological systems. The Institute for Computational and Mathematical Engineering (ICME) was established to teach computational mathematics in the context of engineering and science applications and to provide a school-wide focus on applying computational methods in all areas of engineering and science. Other programs initiated during Dr. Plummer's tenure include the Hasso Plattner Institute of Design, which is known globally for its hands-on, product-centered approach to education, and the Global Climate and Energy Project (GCEP), which has provided resources to boost research in alternative energy. During Dr. Plummer's tenure, other innovations in the Engineering School include the development of online education courses and technologies, including the "flipped classroom model," where video lectures are viewed by students at home before the classroom session to allow focus on exercises and discussions while in class, as well as the world's first massively open online courses (MOOCs) to provide unlimited participation and open access to learning through the Internet. Dr. Plummer's contributions to Stanford's School of Engineering have been instrumental in

increasing the number of students choosing engineering majors, especially in computer science, product design, and bioengineering.

An IEEE Fellow and member of the U.S. National Academy of Engineering, Dr. Plummer holds the John Fluke Professorship in Electrical Engineering at Stanford University, Stanford, California, USA.



Dimitri Antoniadis of the Massachusetts Institute of Technology has been named the recipient of the 2015 IEEE Jun-Ichi Nishizawa Medal. His citation states, "*For contributions to metal oxide semiconductor field-effect transistor physics, technology, and modeling.*"

Known for his deep understanding of device physics, Dimitri Antoniadis has made pioneering contributions to the direction of the integrated circuit (IC) microelectronics industry by advancing the capabilities of metal oxide semiconductor field-effect transistors (MOSFETS). MOSFETs are used for amplifying and switching signals, and today's microprocessors and memory devices contain billions of them. In 1978 while at Stanford University, Dr. Antoniadis developed the SUPREM process simulator, which was the first computer-aided design tool for silicon semiconductor devices and ICs. SUPREM became the preeminent simulator used by practically all IC manufacturers. His work on deep submicron MOS devices during the 1980s was one of the first demonstrations of nano-scale MOSFETs, and his innovations have continued to the foundation of today's high-performance silicon FETs. At MIT, Dr. Antoniadis' groundbreaking research in 1985 proved the feasibility of sub-100-nm MOSFETs and provided the first demonstration of source-to-channel electron injection velocities exceeding saturation velocity. Known as "velocity overshoot," this provides an increase in current drive in short-channel MOSFETs, enabling higher performance previously not thought attainable. His development of the virtual-source model to describe the behavior of very short channel devices has shown the role of high carrier velocity and mobility in obtaining maximum device performance. With the ability to accurately simulate the characteristics of MOSFETs down to 22 nm and beyond, the model has been adopted by the International Technology Roadmap for Semiconductors (ITRS) for predicting the future of MOSFET scaling. As director for twelve years of the Materials, Structures, and Devices Center, Dr. Antoniadis has helped determine the most promising path for future microelectronics by pursuing scaling of MOS to its ultimate limit and interdisciplinary exploration of new-frontier devices.

An IEEE Life Fellow and member of the U.S. National Academy of Engineering, Dr. Antoniadis is currently a professor and the Ray and Maria Stata Chair in Electrical Engineering at the Massachusetts Institute of Technology, Cambridge, Massachusetts, USA.

Paul Yu
EDS Awards Chair
University of California at San Diego
San Diego, CA, USA

2015 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award Winners

The 2015 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award was presented to Professor Roger T. Howe, Stanford University and Dr. Yu-Cong Tai, California Institute of Technology, at the 2015 Transducers Conference in Anchorage, Alaska on June 22, 2015. This prestigious award recognizes and honors advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices.

Roger T. Howe

For sustained contributions to MEMS/NEMS over many years especially those enabling MEMS-based inertial-sensor applications

Roger T. Howe is the William E. Ayer Professor in the Department of Electrical Engineering at Stanford University. He received a B.S. in physics from Harvey Mudd College and an M.S. and Ph.D. in electrical engineering from the University of California, Berkeley in 1981 and 1984. After faculty positions at Carnegie-Mellon and MIT from 1984–1987, he returned to Berkeley where he was a Professor until 2005. His research interests include MEMS and NEMS design, fabrication technologies, and applications in energy conversion and biosensing.

He served as Co-General Chair of the IEEE MEMS Workship in 1990 and was the Technical Program Chair of Transducers 2003 and is an editor of IEEE JMEMS. He was elected an IEEE Fellow in 1996, was co-recipient of the 1998 IEEE Cledo Brunetti Award, and was elected to the U.S. National Academy of Engineering in 2005 for his contributions to MEMS.

Yu-Cong Tai

For pioneering contributions in materials, technologies, and design of MEMS/NEMS and groundbreaking achievements in the realization of biomedical parylene MEMS

Yu-Chong Tai (M'96-SM'03-F'06) is the Anna L. Rosen Professor of Electrical Engineering and Mechanical

Engineering at Caltech. He also serves as the first Executive Officer of Caltech's newly formed Medical Engineering Department, where the goal is to leverage today's cutting-edge technologies in order to make possible major improvements in medical diagnostics and treatment. Professor Tai played a seminal role in the formation of this department.

Professor Tai received his B.S. degree in Electrical Engineering from National Taiwan University in 1981, and M.S. and Ph.D. degrees in EECS from the University of California, Berkeley in 1986 and 1989, respectively. In groundbreaking doctoral research at Berkeley, Tai and co-workers demonstrated means to build springs, sliding elements, gears, and ultimately an operating rotational electric micromotor using polycrystalline silicon. In 1989, Dr. Tai joined Caltech as an Assistant Professor in Electrical Engineering. In his research at Caltech, Professor Tai and his group have produced pioneering and outstanding results in research supporting micro-fluidic MEMS, lab-on-a-chip systems, and micro implantable biomedical devices

Dr. Tai served as co-chairman of the 2002 IEEE International MEMS Conference. He was elected an IEEE Fellow in 2006, and is a senior member of the American Society of Mechanical Engineers (ASME).

Richard Muller
EDS Bosch Award Chair
University of California, Berkeley
Berkeley, CA, USA

IEEE Nanotechnology Council Announces 2015 Award Winners

The IEEE Nanotechnology Council Awards Committee (Chaired by Prof. Joe Lyding) has announced its 2015 award winners for the IEEE Nanotechnology Pioneer Award, and the IEEE NTC Early Career Award. These awards were presented July at the IEEE NANO 2015 in Rome, Italy.

Pioneer Award in Nanotechnology
Professor Chennupati Jagadish
Distinguished Professor and Head of Semiconductor Optoelectronics and Nanotechnology Group
The Australian National University
Canberra, Australia
chennupati.jagadish@anu.edu.au

"For pioneering and sustained contributions to compound semiconductor nanowire and quantum dot optoelectronics."

Early Career Award
Professor Deji Akinwande
Assistant Professor of Electrical and Computer Engineering
University of Texas at Austin
deji@ece.utexas.edu

"For pioneering contributions towards the understanding and development of wafer-scale graphene and flexible nanoelectronics based on two-dimensional sheets."

Congratulations to the award winners!

Joe Lyding
2015 IEEE NTC Awards Committee Chair
University of illinois
Urbana, IL, USA

Announcement of the 2015 EDS PhD Student Fellowship Winners

Carmen M. Lilley
EDS Student Fellowship Committee Chair

The Electron Devices Society PhD Student Fellowship Program was designed to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest.

EDS proudly announces three EDS PhD Student Fellowship winners for 2015: **Shahab Akhavan** – Bilkent University, Ankara, Turkey, **Der-Hsien Lien** – National Taiwan University, Taipei, Taiwan, and **Max Shulaker** – Stanford University, Stanford, California, USA. Brief biographies of the recipients appear below. Detailed articles about each PhD Student Fellowship winner and their work will appear in forthcoming issues of the EDS Newsletter.

Shahab Akhavan received his B.Eng. degree in Materials Science and Engineering in 2010 at Middle East Technical University and his M.S. in Materials Science and Nanotechnology in 2013 at Bilkent University. Currently, he is pursuing his PhD at Bilkent University under the supervision of Prof. Dr. Hilmi Volkan Demir. Shahab Akhavan has published 10 research articles in major peer-reviewed scientific journals (6) and international conferences (4), and he has currently holding one patent. He is serving to the scientific community as a reviewer of Small, Optics Express, Optics Letters and Optics Materials Express. He is working on the fabrication of a new generation of light-harvesting devices along with the scope of introducing new concepts into optoelectronic devices based on colloidal nanomaterials.

Der-Hsien Lien received B.S. degree and the M.S. degree in the Department of Materials Science and Engineering from National Tsing Hua University. He is a Ph.D. student in the Institute of Electronics Engineering at National Taiwan University (from 2012), and currently works in the Electrical Engineering & Computer Sciences, UC Berkeley as a visiting scholar (from 2014). His research interests include the nanophotonics dynamics and applications, 2D materials electronics and photonics, random access resistive memories, and flexible optoelectronics. Currently he has authored 35 peer-reviewed journal papers, h-index of 12 and 704 citations, holds 1 US patent and 2 Taiwan patents.

Max Shulaker is a PhD candidate in Electrical Engineering at Stanford University, under the supervision of Professor Subhasish Mitra and co-advised by Professor Philip Wong. He received his B.S. from Stanford University in Electrical Engineering. Max's current research interests are in the broad area of nanosystems. His research results include the demonstration of the first carbon nanotube computer, the first digital subsystems built entirely using carbon nanotube FETs, the first monolithically-integrated 3D integrated circuits combining arbitrary vertical stacking of logic and memory, and the highest-performance CNFETs to-date. These works drastically altered the status-quo of these emerging nanotechnologies, as they are the first system level demonstrations among these promising emerging nanotechnologies, the most complex carbon-based digital systems ever demonstrated, and the first experimental demonstration of one of these emerging technologies competing with the drive-current of silicon-based transistors available from commercial foundries.

Carmen M. Lilley
EDS Student Fellowship Committee Chair
University of Illinois at Chicago
Chicago, IL, USA

Congratulations to the 14 EDS Members Recently Elected to IEEE Senior Member Grade!

Sergio Camacho-Leon
Malcolm Carruthers
Gabriel Cormier
Joseph Daniele
Saverio Fazzari*
Jonathan Felbinger*
Ning Ge
Qun Gu
Sefer Bora Lisesivdin
Krishna Mandal
Romualdas Navickas
Akira Satou
Takatoshi Tsujimura
To-Po Wang

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US$25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application: https://www.ieee.org/membership_services/membership/senior/application/index.html.

You will need to Sign-in with your IEEE account.

Please remember to designate the Electron Devices Society as your nominating entity!

EDS Membership Fee Subsidy Program

Applications Now Being Accepted for 2016

Mikael Östling
EDS Vice-President of Membership & Services

Our society continually works to increase the value of EDS membership and our colleagues enjoy an incredible array of free and deeply-discounted, members-only benefits. One EDS initiative to encourage newcomers and assist current members is the **EDS Membership Fee Subsidy Program** (MFSP). This program offers the generous incentive of one year complimentary IEEE and EDS memberships to help launch new chapters or enable existing ones, in low income geographical areas to grow their memberships.

This special offer is available to students and to those professionals who meet the eligibility requirements.

To complement our Society program, we are encouraging members in eligible countries to try IEEE e-Membership (an electronic membership option with reduced fees). Please visit the IEEE website for more details on e-Membership: http://www.ieee.org/membership_services/membership/join/emember.html.

The EDS Membership Fee Subsidy Program policy is as follows:

- EDS will cover the cost of a full year of IEEE and EDS membership for up to 15 new or current members per chapter, provided the existing members have not received MFSP benefits in the past.
- **Five** of the fifteen members each year must be new IEEE/EDS members.
- New and renewing members must apply through their local chapter. Current elected officials of eligible EDS chapters will receive instructions from the EDS Executive Office.
- Chapter Chairs must verify member's eligibility according to IEEE income guidelines.

Please visit the EDS website for more information on the EDS Membership Fee Subsidy Program: http://eds.ieee.org/mfsp.html. Any questions should be directed to Joyce Lombardini (j.lombardini@ieee.org), EDS Membership Administrator.

Mikael Östling
EDS Vice-President of Membership & Services
KTH, Royal Institute of Technology
Sweden

Call for Nominations for Editor-in-Chief IEEE Journal of the Electron Devices Society

The IEEE Journal of the Electron Devices Society (J-EDS) is an open access, fully electronic scientific journal publishing papers ranging from fundamental to applied research that are scientifically rigorous and relevant to electron devices. J-EDS publishes original and significant contributions relating to the theory, modeling, design, performance and reliability of electron and ion integrated circuit devices and interconnects, involving insulators, metals, organic materials, micro-plasmas, semiconductors, quantum-effect structures, vacuum devices, and emerging materials with applications in bioelectronics, biomedical electronics, computation, communications, displays, microelectromechanics, imaging, micro-actuators, nanoelectronics, optoelectronics, photovoltaics, power ICs and micro-sensors. J-EDS publishes regular full-length papers, review papers, invited papers, and special issues. It provides authors an affordable outlet for rapid publishing and universal access.

We invite nominations for the position of Editor-in-Chief (EiC) for J-EDS for a 3-year term starting in 2016. The EiC's duties include appointing Editors to serve across the scope of the journal; supervising the operations of the journal through ScholarOne Manuscripts with the assistance of the EDS publications staff; monitoring the quality and timeliness of publications; and leading development to strengthen the journal.

Criteria for the Nominees:

- Demonstrated competence in at least one of the disciplines included in the EDS field of interest;
- Ability and motivation to spend sufficient time on the job;
- Formal support from the institution for which the nominee works (waived if self-employed);
- Has served or currently is serving on one of the editorial boards of T-ED (the IEEE Transactions on Electron Devices), EDL (the IEEE Electron Device Letters), or J-EDS;
- Suitable temperament (ability to work at all levels: editorial boards, IEEE/EDS staff, volunteers, authors, reviewers, officers, etc.) and judgment;
- Be a member of EDS;
- Other desirable qualifications include leadership experience, integrity and ethical standards, organizational and management skills, and a vision for moving the journal to a new level of excellence.

Requirement for Nominations:

- A brief IEEE-style biography (up to 250 words) of the nominee;
- A complete CV and list-of-publications of the nominee;
- A brief statement from the nominator on nominee's qualification and how the nominee meets the criteria listed above;
- A letter from nominee's employer indicating support for the EiC activity;
- No specific requirement on the nominators and self-nominations are permissible;
- Endorsement from two EDS members on the nomination;
- Optionally, a statement (up to 500 words) from the nominee on his/her vision for the journal.

Please email the nomination materials to: Marlene James (m.james@ieee.org) by November 15, 2015.

Bin Zhao
VP of Publications and Products
IEEE Electron Devices Society

Announcing a new website for the IEEE/OSA Journal of Lightwave Technology, www.ieee-jlt.org

The new website contains:

- Highly cited and frequently downloaded JLT papers
- Featured JLT Special Issues, like ECOC 2014
- Winners of the JLT Award with free open access to the winning papers
- Recent noteworthy JLT papers
- JLT Special Issues - Browse by year or by topic area
- Call for Papers for upcoming JLT Special Issues
- Answers to frequently asked questions on such topics as JLT review times, open access publication options, and ArXiv posting
- Who is who on JLT's Editorial Board — Staff, and Steering/Coordinating Committee

Happy Browsing!

Young Professionals

Reflections from Young Professionals

Our second article/interview on *"Reflections from Young Professionals"* is featuring Daniel Camacho, Chairman of the EDS Young Professionals Committee and an elected member of the EDS Board of Governors. As a young professional working in industry his views and perceptions about IEEE and EDS are of significance. Newsletter Editor-in Chief, MK Radhakrishnan has interviewed Daniel Camacho and the excerpts of the interview are given here.

Daniel Camacho

Editor: As an young professional in the early age of your professional career, why do you consider the membership in IEEE and especially in EDS is important?

Daniel: Being a member of IEEE and EDS is relevant at many different levels. Let's start mentioning the ones that are self-evident. IEEE, and EDS by extension, has one of the largest collections of technical papers in the world. Additionally, they sponsor some of most important engineering conferences in the world, like our own IEDM, and they provide a discount for its members to participate on them. Furthermore, EDS has a marvelous Webinar program that allows its members to have first-hand access, anywhere in the world, to some of the biggest experts in EDS' fields of interest. Those are by itself are very compelling reasons to be part of IEEE and EDS, but for me the real deal breaker is the people. The opportunities to connect with other engineers with similar interests as well as the chance to build a network of contacts that could include senior engineers that are willing to mentor you in your career is something you cannot really put a price on.

Editor: What was the specific temptation, if any, which made you to join this largest professional organization in the globe at first, and become an elected member of EDS Board of Governors?

Daniel: I have been an IEEE and EDS member for quite some time now, I first joined by the end of my college years, I was sure IEEE and EDS were going to be relevant for my professional development, for both the technical aspects as well as for the networking opportunities. Looking back I did not really understood the magnitude of the decision, EDS has become a huge part of my career and one I feel very proud of. Back in 2008, I received one of the EDS Student Fellowship, and at this point, I am fully convinced that the award helped me to open doors for my professional development. As a result I felt that it was only fair to give back to EDS as way to thank for what I have received for my involvement with the society. So when the opportunity to participate in the election, and become part of the EDS Board of Governors appeared, I immediately jumped into it.

Editor: As a Professional, how do you position your interest in your own technical field with the activities and services you perform as an EDS member/volunteer?

Daniel: Funny enough my line of work has deviated slightly from EDS field of interest, is not entirely separated, but if it were because of my day-to-day work I would probably had to jump into a different society. However, I do not find that to be an issue, on one hand I still have the right background to be "technically relevant" – for the lack of a better term- for the society; and on the other hand volunteering for EDS goes much more further than just technical activities. In fact I think that for YP the non-technical activities are the ones that bring the bigger return of inversion for YP. For example, we have organized Webinars for YP on topics like the advantage of Grad School, or what to expect of working in the Industry, activities that in my opinion have a great value for the YP, but require almost no technical background. In other words, I think I have found the right balance and the right way to volunteer and serve the society regardless of my daily technical activities.

Editor: What are your thoughts about the EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth? If so, how?

Daniel: Young Professionals tend to overlook the importance of networking. For some reason, we tend to believe that excelling in the technical stuff will be enough to open all the doors however that is far from the reality. I cannot stress enough the importance of networking,my admission to grad school, my first job, and the opportunity to volunteer in EDS have all come as a result of effective networking. Most of my networking occurs inside EDS, and is there where I learned how to actually do it. The society has been a tremendous support for my career, and as a YP myself, I have run into a wonderful group of professionals who have helped me navigate the first years of my professional life in a way that I like to consider successful.

Editor: As a YP, how do you consider the ED Society as a whole and what are the changes or developments you would like to see in evolving this professional body as a group devoted to the humanity and its causes?

Daniel: The semiconductor industry is probably the most rapidly evolving industry in the history of humankind. EDS has to be capable of adapting to the industry as it evolves and transforms itself, as challenging as it sounds, is imperative for the society to keep up the pace, and to even lead it when there is the opportunity to do it. However, in order to do so, I believe we are in need of younger active volunteers that can help shape the EDS of tomorrow. Unfortunately, is easier said than done, and we still need to find a path to get YP much more actively involved.

Editor: What are your suggestions and recommendations for those young professionals who may aspire to join EDS?

Daniel: The first and foremost thing I can suggest is to join as soon as possible, stop contemplating the options, and start right away, there is nothing to lose and lots to gain. Once you have joined, there are two things you need to start doing, maximize your membership by attending webinars and EDS events in your area, also start connecting to people, talk to them and figure out how do your interests align with theirs, that will open the doors to volunteering and growing your career. EDS needs you, and we hope we can give you in return for your volunteering a path to a better professional career.

Daniel Camacho *is an electrical engineer with vast industry experience in the field of analog and mixed signal integrated circuit design in the most advanced fabrication nodes. He obtained his Bachelor's degree in 2007 from Pontificia Universidad Javeriana in Bogota, Colombia. His Masters Degree was conferred in 2009 by Southern Methodist University, in Dallas, Texas. In 2008 he was awarded the EDS Masters Student Fellowship for his research work in EDS fields of interest. In 2010 he joined Intel Co. as an analog design engineer, and has remained with the company since then.*

He has been an active volunteer of EDS since 2009, as member of the Young Professional committee, and later as its chairman. In 2012 he was elected as the Young Professional member of the EDS Board of Governors.

XII National Meeting of Student Branches and III National Meeting of Young Professionals

Jacobus Swart, SRC Region 9 Chair

The event took place at the University of Brasilia, Brazil, June, 4-7, 2015, and is held annually in Brazil with participation of many student branches and session chairs. This year it received participation of IEEE past president, Roberto de Marca, as well as other key members of IEEE and its societies from around the world. The main topic of this year's event was *"Challenges and Perspectives of Engineering in Brazil and the role of IEEE on professional workforce and labor market."* Jacobus Swart participated as SRC Chair for IEEE Region 9 and delivered an EDS Distinguished Lecture entitled, *"Challenges and Perspectives of Semiconductor Engineering in Brazil."* More than 120 people attended the lecture, most of them students. More information can be found on the event website at, http://rnr2015.com.br and in a report at, https://drive.google.com/file/d/0B–MCtnoxod8VIY5RnNHUDhnUFU/view.

Group picture after the EDS Distinguished Lecture, (J. Swart in white shirt on left)

QuestEDS

Samar Saha
EDS President-Elect

Interested in knowing why it's not possible to measure the built-in voltage of a PN junction using a voltmeter? Do you need to understand the best way to derive an expression for the average thermal velocity of an electron? Or are you curious about what quantum dots and wires are? The answers to these questions and more are available through the QuestEDS Question and Answer page.

To ask a question not already addressed on the Q&A page, visit www.ieee.org/go/questeds. Technical experts answering the questions posed represent academic, government, and industry sectors.

Questions are grouped into nine technical categories and two general ones. Technical categories cover subject areas like semiconductor and device physics, process technology, device characterization, technology CAD, compact modeling, VLSI interconnects, photovoltaics, and quantum electronics. Subject areas addressed are anticipated to expand in the future. Two other categories address questions pertaining to educational activities and general inquiries about society membership. Within a two week time frame from when the question is asked, an answer is posted online. Incoming questions are handled by an editor-in-chief who ensures that they fall within the technical scope of EDS and that they are adequately answered.

To view the entire library of questions and answers, visit http://eds.ieee.org/member-sign-in-form.html?notauth=1. Your IEEE login is required to view the answer page.

Organic Semiconductor Devices

Question 060-13:
Considering that an organic semiconductor, such as "Tips-pentacene", was spin-coated on top of an aluminum sheet, sintered and subjected to a final 3rd layer of gold (applied using a square shadow mask), what would be an appropriate set of formulas that would predict the current dynamics as a function of the voltage and geometry of the layers in this schottky device? If the same experiment were performed, but this time applying the tips-pentacene by drop-cast, how should expectedly vary the results? Does the rugosity of the layers affect the performance of the device? Why should one consider the rugosity relevant?"

Answer 060-13:
Generally, to fabricate the vertical organic diodes, it is preferred to coat TIPS-pentacene on the top of Au, and then evaporate Al on the top of the TIPS-pentacene, since Al surface is very easy to oxidize. Typically, the Al/TIPS interface forms a large barrier for injection of holes from Al into the HOMO level of TIPS-pentacene. In contrast, Au electrode has a very low barrier for injection of holes into the HOMO level of TIPS-pentacene. Therefore, assuming perfectly injecting ohmic contacts of Au electrode with TIPS-pentacene, the forward-biased current (flowing from the Au electrode to the Al electrode) can be described by the space-charge-limited current density [1]. The reverse-biased current can be described by Schottky diode reverse current model [2]. The main difference to the classical Schottky diode theory is that the organic semiconductor layer is always fully depleted due to the very low carrier density, and thus the devices could show a voltage-independent, constant reverse-bias capacitance [3].

For solution processed TIPS-pentacene devices, the different coating processes could form thin films with different crystalline structures, which then affect the contact properties and bulky trap states. Therefore, the electrical characteristics could be influenced. Currently, there have been very few experimental studies on solution processed organic small molecule diodes, and this area is worth further investigation.

References:
[1] M. Raja, et al., "Modelling of polymer Schottky diodes for real device applications," Proc. of ESSDERC, 2005, pp. 253–256.
[2] S. Steudel, et al., "50MHz rectifier based on an organic diode," Nature Materials, vol. 4, no. 8, pp. 597–600, Aug. 2005.
[3] C.H. Kim, et al., "Capacitive behavior of pentacene-based diodes: quasistatic dielectric constant and dielectric strength," J. Appl. Phys., vol. 109, no. 8, pp. 083710-1–083710-9, Apr. 2011.

Samar Saha
EDS President-Elect
Prospicient Devices
Milpitas, CA, USA

EDS-ETC
Engineers Demonstrating Science: an Engineer Teacher Connection

University of Brasilia Student Chapter – wins the 2015 Darrel Chong Student Activity Award!

Luiz Fernando de Andrade Gadêlha
Coordinator of Projeto Electron/IEEE/UnB

Congratulations to the University of Brasilia Student Chapter on winning the 2015 Darrel Chong Student Activity Award. *For demonstrated steps toward improving the quality of IEEE Student Activities and the fostering of knowledge sharing.*

The Project Electron program is a volunteer activity of the University of Brasilia (UnB) IEEE Student Branch. Its objective is to encourage public school students to pursue engineering as their professional career, and the project teaches basic electronics using Snap Circuits Kits and Arduino, donated by the IEEE Electron Devices Society.

Dynamic and fun classes are taught by graduate students, so that public school students view exact sciences with other eyes, not thinking it is difficult and tiring, but interesting and attractive. Unlike the common classes, where students just sit and listen to the teacher, in the Electron Project they have the chance to learn by exploring and discovering, just treading their own path of learning. Teaches values and practices for students who participate as a volunteer instructor, helping them to develop skills little contemplated in engineering courses, such as communication, organization and adaptation.

University of Brasilia Student Chapter team

In 2014, Project Electron workshops were held in even more public schools than before and the program has focused its activities to impact girls to follow engineering.The project was assisted in that objective by the IEEE UnB Women in Engineering (WIE) group. Chapter currently has 15 volunteers as a result of these program's growth and recognition. The student volunteers participating in the project will receive grants from Deanship Extension of UNB (DEX) and the Ministry of Education (MEC), a result of the announcement PROEXT 2014. A selection process among interested students to participate was conducted by checking the specific skills of each to growth of this project. With the increase of student volunteers, other institutions are being evaluated for participation in the program in the future.

Of the three new public schools and two charitable organization programs set up, about 60 students were directly impacted by the project and hundreds indirectly. Many students decided to follow engineering because of Project Electron and some who participated in high school opted to do an engineering course and enrolled at the University.

EDS-ETC Report from the AP/ED/MTT/COM/EMC Tomsk Chapter

Oleg Stukach, Vice Chair of Tomsk Chapter

The Chapter used a new approach for the utilization of EDS-ETC Snap Circuits Kits. This year for the first time the Chapter employed the "Open Door Days" of the Institute of Cybernetics of Tomsk Polytechnic University (TPU) for Snap Kit demonstrations among school children. Normally this event promotes training programs and curriculum description of the Institute for fresh students who intend to join the University in summer. Majority of the school children can apprehend information only in the game form. It is the result of relation to the engineering education. The Snap Circuits kits were used to demonstrate physical laws and simultaneously the practical applications, which was demonstrated this year with the full involvement of students. The children responded very positively by asking various questions related to electronics engineering during the session. Thus, these gadgets helped to provide more practical knowledge and to show the engineering subject is more interesting. Since the beginning of 2015 the Chapter has held three high-grade meetings of this nature, and plan to continue this type of program.

School children practicing utilizing the Elenco Snap Circuits© Kit

ED Calcutta Chapter EDS-ETC Program

The ED Calcutta Chapter with active support from the student members of the ED University of Calcutta Student Branch Chapter organized an EDS-ETC Program on March 31, 2015 at 'Brahmo Balika Shikshaloy.' A total number of 16 projects were carefully selected and demonstrated to the students with the help of the Elenco Snap Circuits® kits. The basic ideas of transistor, solar cell, digital logic gates were explained to the students by the EDS University of Calcutta Student Branch Chapter.

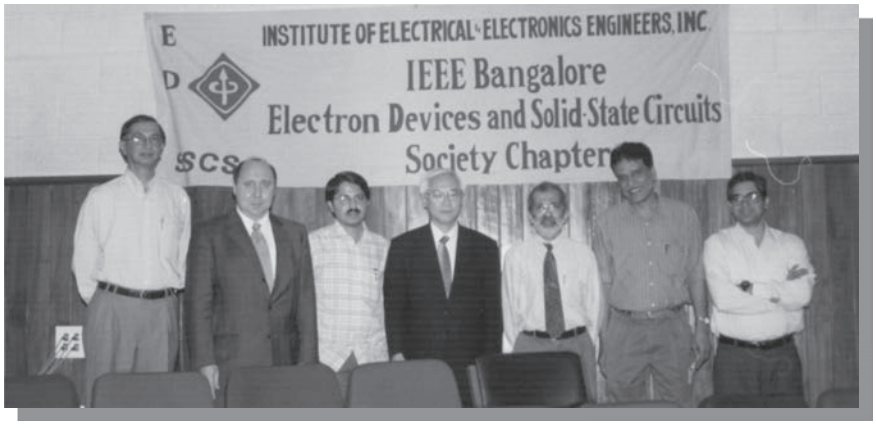
EDS-ETC program held at Brahmo Balika Shikshaloy

Chapter News

Growth of a Chapter and its Reflections in the Society

By Navakanta Bhat
IISc, Bangalore, India & ED/SSC Bangalore Chapter

One of the most active EDS chapters in Region 10, the IEEE ED/SSC Bangalore Chapter, has about 230 members of which more than 150 members are from the Electron Devices Society. The EDS membership has witnessed an impressive growth from a mere 17 EDS members at its inception in October 2001, indicating an average annual growth rate of about 17%. The quality and quantity of the programs organized by the chapter and hard work put in by the ExCom members and volunteers are the secrets behind this growth. I have had the opportunity to associate with the chapter from its formative years, first as the founding chair, and then as an ExCom member volunteering in various technical activities. Based on my experience in the Bangalore region, touted as the Silicon Valley of India, I strongly feel that the EDS membership can continue to grow at this pace for several years to come, as there is plenty of untapped resource pool. Hence it is an opportune time to reflect on the genesis and evolution of the chapter, and share the best practices with rest of the EDS community at large, and thereby plan for future growth.



J. Vasi, C. Claeys, N. Bhat, H. Iwai, M.K. Radhakrishnan, K. Rajagopal and Mahesh Patil at the one day workshop, as a formal inauguration of the IEEE ED/SSC Bangalore Chapter, on March 16, 2002

Prof. Juzer Vasi (IIT Bombay), Prof. Renuka Jindal (UL Lafayette), Prof. Hiroshi Iwai (Tokyo Institute of Technology), and Dr. M. K. Radhakrishnan (NanoRel) played a crucial role in catalyzing the formation of the ED/SSC Bangalore Chapter in 2001. They also helped as Chapter partners in the early years. As the future semiconductor technology required a very strong coupling between chip design and underlying device physics and process technology, such as the process variability and its impact, it was a logical choice to anchor the joint chapter with both EDS and SSCS societies. The presence of several multinational chip design companies having research and development centers in Bangalore provided an opportunity to enhance the membership base. The chip design industry ecosystem nicely complemented the strong research base in electron devices, materials science and process technology at the Indian Institute of Science (IISc) – the oldest graduate research school in India. IISc also acted as a host to most of the Chapter events and continues to do so even today.

Obtaining the formal approval from IEEE HQ in October 2001, the Chapter started conducting events immediately thereafter – on an average one technical talk per month initially. We took a conscious decision to keep all the events free for members and non-members alike, and this turned out to be a good strategy to entice non-members to join IEEE and EDS. The formal inauguration of the chapter was held on March 16, 2002, by conducting a one-day workshop consisting of several EDS DL seminars, with the participation of more than 100 attendees. The chapter ExCom also set a goal to scale up the activities aimed at professionals.

Also, in 2002, the chapter started conducting several events outside IISc, to enhance the reach around Bangalore. The senior members of the chapter initiated technical workshops in engineering colleges, which encouraged students and faculty to become EDS members. We also started scheduling technical talks by experts in industry premises in Bangalore – such as Texas Instruments and National Semiconductors, to name a few. Further the chapter decided to cooperate with the VLSI

ICEE 2014 organized by the ED Bangalore Chapter

Society of India to conduct the annual three-day technical event on VLSI Design and Test workshop (VDAT). Due to the active participation of the chapter members in such programs over the next couple of years, a substantial emphasis on electron devices technology was also brought into the scope and deliberations of these workshops.

In the next few years, the chapter decided to expand its activities beyond Bangalore city. The volunteers started conducting technical talks and workshops in neighboring cities such as Mysore. This helped a lot in expanding the EDS base. For instance, the EDS student chapter in SJCE, Mysore, the first such student chapter in the Region, was formed and is one of the most vibrant student chapters today. The EDS Bangalore Chapter also helped mentor the EDS Kolkota Chapter. Also, the chapter started working together with other IEEE chapters in Bangalore such as CAS and CPMT, to broaden the scope of topics, for the benefit of members. This included "Bridging technology and design in nanometer era," and "Reliability of Nanodevices and circuits." The EDS lending library was utilized efficiently, to screen several IEDM courses for the benefit of members. The contributions made by the Bangalore chapter were well recognized through the Outstanding Chapter of the Year award by the SSC society in 2003 and by the ED society in 2005.

In 2007, the chapter successfully organized the IEEE International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA). The conference was very well attended with the participation of more than 300 delegates. This also helped enhance the visibility of the chapter among the international community. During the subsequent years, events such as DL colloquium and WIMNACT became an integral part of the calendar of events. The Bangalore chapter took initiatives to coordinate meetings among various chapters in the South Asia region. During one such meeting held in Bangalore, it was decided to initiate a biennial conference on electron devices promoted by EDS South Asia Chapters to benefit the professional community. A working group from the ED Bombay and ED Bangalore chapters was entrusted, to plan and initiate the conference series, ICEE (International Conference on Emerging Electronics). The first ICEE conference was conducted at IIT Bombay in 2012, jointly organized by the IEEE EDS Bombay and Bangalore chapters. The conference was very well attended with about 300 delegates. The second conference was held in December 2014, at the Indian Institute of Science Bangalore, jointly organized by the ED Bangalore and Bombay chapters (http://www.cense.iisc.ernet.in/icee/). This conference was attended by about 500 delegates and has set a momentum for subsequent conferences to follow. ICEE conference has already emerged now as a key event of international repute. With the next few editions of ICEE, we expect it to emerge as a "go-to event" in the electron devices field.

Since the inception in 2001, the ED Bangalore Chapter has established itself as one of the vibrant chapters serving the community. It should be instructive to appreciate the current ecosystem around the ED Bangalore chapter and recognize future opportunities. The electron devices community in the region is growing at a very rapid pace, due to several interventions from the Government of India. With the launch of National Nanoelectronics Initiative in India in 2005 and with the creation of several centers of excellence with Nanofabrication capabilities, the growth of the electron devices field has seen a tectonic shift in the country. For instance, the National Nanofabrication Centre at IISc (www.cense.iisc.ernet.in), Bangalore boasts world class research facilities for electron devices, materials and processes. Indian Nanoelectronics Users Program-INUP, an innovative network program has enabled unprecedented growth in the device community (http://www.nano.iisc.ernet.in/inup/). Bangalore has become the home for the India Electronics and Semiconductor Association-IESA (http://www.iesaonline.org/). SEMI has also setup its operations in Bangalore, to work with all stake holders and nurture and grow the semiconductor ecosystem. In fact, the ED Bangalore Chapter has contributed in a subtle way for such a cascade of events in Bangalore. It is a good example illustrating the fact that the growth

and contributions of a Chapter can be beneficial to the society at large.

Navakanta Bhat *is a Professor in the Centre for Nano Science and Engineering and Electrical Communication Engineering Department, Indian Institute of Science, Bangalore. He received M.Tech from I.I.T. Bombay in 1992 and Ph.D. from Stanford University in 1996. Prior to joining IISc in 1999, he worked at Motorola's Advanced Products R&D Lab in Austin, Texas. His current research is focused on Nanoelectronics technology and Integrated CMOS-MEMS sensors. He has more than 200 journal publications and 20 patents to his credit. He was instrumental in the formation of National Nanofabrication Centre (NNfC) at IISc, Bangalore, benchmarked against the best university facilities in the world, and serves as the chairman of NNfC administration committee. He is a recipient of many awards including INAE Young Engineer Award (2003) Swarnajayanti fellowship (2005) from Department of Science and Technology, Govt. of India and Prof. Satish Dhavan award (2005), IBM Faculty Award 2007 and Outstanding Research Investigator Award (2010) from DAE. He was the founding chair of the IEEE ED/SSC Bangalore Chapter and was an EDS DL. He is the Editor of IEEE Transactions on Electron Devices, a Fellow of the Indian National Academy of Engineering and senior member of IEEE.*

MQ and Conference Reports

ED Malaysia Kuala Lumpur Chapter

By Badariah Bais & Zubaida Yusoff

DL Mini – Colloquium (MQ) at UKM

On May 29, 2015, the IEEE ED Malaysia Chapter organized the '2015 Mini-Colloquium' at the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia. The event started with an introduction of the IEEE Electron Devices Society by IEEE EDS Distinguished Lecturer (DL) and IEEE Electron Devices Society Secretary, Dr. Fernando Guarin. In his introduction, Dr. Guarin talked about the IEEE Electron Devices Society and he reminded us on how device technology has helped to improve our life today. The event was then followed by three talks by IEEE EDS DLs.

Participants of the DL MQ program at IMEN, UKM, Malaysia

The first lecturer, Dr. M.K. Radhakrishnan from NanoRel Technical Consultants gave a talk on '*Interface Physics in Silicon Nanodevices.*' Dr. Radha emphasized that the understanding of physical phenomenon, especially on the interface and interconnect interface with which the devices malfunction, is very important to improve the device reliability. The second lecturer, Dr. Mukta Farooq from IBM Systems and Technology Group presented a talk entitled, '*3 Dimensional Integration Technology.*' In her talk, she explained 3D die stacking integration technology

using a Through Silicon Via (TSV). This technology is able to enhance system performance by increasing bandwidth, reducing wire delay, and improved power management.

The last talk presented by Dr. Fernando Guarin, who is also from IBM Systems and Technology Group, was on *'Trends in Technology, Reliability and Qualification of Leading Edge CMOS Technologies.'* Dr. Guarin addressed some reliability issues driven by the leading edge technologies such as High K Metal Gate (HKMG) and FinFet devices. About 30 participants attended the mini-colloquium. The event ended with the presentation of tokens of appreciation by the IEEE ED Malaysia Chapter Chair, Assoc. Prof. Dr. Badariah Bais, to the three EDS Distinguished Lecturers.

IEEE EDS Mini-Colloquium – Ireland and University of Manchester Student Chapter

By Ali Rezazadeh
Chair of IEEE R8 AP/ED/MTT/PHO UK and Ireland Chapter

The IEEE Region 8 UK and Ireland AP/ED/MTT/PHO Chapter and the University of Manchester IEEE EDS Student Chapter co-hosted an IEEE EDS sponsored mini-colloquium at the University of Manchester in April 2015. The theme of the MQ was "*Advances in Semiconductor Devices and 3D Integration*" and comprised presentations from three invited IEEE EDS Distinguished Lecturers and one local speaker from the University of Manchester. Over thirty delegates, including postgraduate students, researchers and lecturers, attended the event, which began with the chairs of the two societies, Prof. Rezazadeh and Mr. Peter Kyabaggu, welcoming the speakers and the delegates. This was followed by an introduction of IEEE EDS activities by Distinguished Lecturer, Dr. Simon Deleonibus of CEA-Leti, France.

The speakers' talks covered advancements in electron devices and the challenges of 3D integration from both academic and industrial points of view. Prof. J. J. Liou of the University of Central Florida, spoke on the "*Outlook and Challenges in Electrostatic Discharge Protection of Modern and Future Integrated Circuits,*" Dr. Simon Deleonibus presented "*The Future of More Moore and More-than-Moore Devices in the Context of 3D Integration,*" and Prof. Benjamin Iniguez of the Universitat Rovira i Virgili, Spain, spoke about "*Physically-Based compact Modeling of AlGaN/GaN HEMTs,*" Local speaker, Prof. Ali Rezazadeh presented *"Challenges and Constrains in Design and Development of Compact 3D MMICs."* Following a working lunch, students of the University gave an interactive poster session highlighting their research activities. The entire stimulating event proved a great success with all those in attendance.

The four MQ speakers (front row, sixth from left), Prof. Benjamin Iniguez, Prof. J.J. Liou, Dr. Simon Deleonibus and Prof. Ali Rezazadeh, with some of the audience members

WIMNACT-47 IEEE EDS Mini-Colloquium at Singapore

By X. Zhou (NTU), Y. C. Liang and C. X. Zhu (NUS), K. Shubhakar (SUTD)

The 47th Workshop and IEEE EDS Mini-Colloquium on NAnometer CMOS Technology (WIMNACT-47) was held in Singapore on June 5, 2015, with 11 Distinguished Lecturers (DLs) participating at 3 local universities. This event was organized and financially sponsored by the EDS Mini-Colloquia (MQ) Program and the R/CPMT/ED Singapore Chapter, immediately following the EDS BoG Meeting and EDSSC 2015 conference, leveraging on the DLs' participation in these events.

After a refreshing morning tour to the Sungei Buloh Wetland for the 11 DLs, they travelled to 3 Universities for parallel MQs in the afternoon.

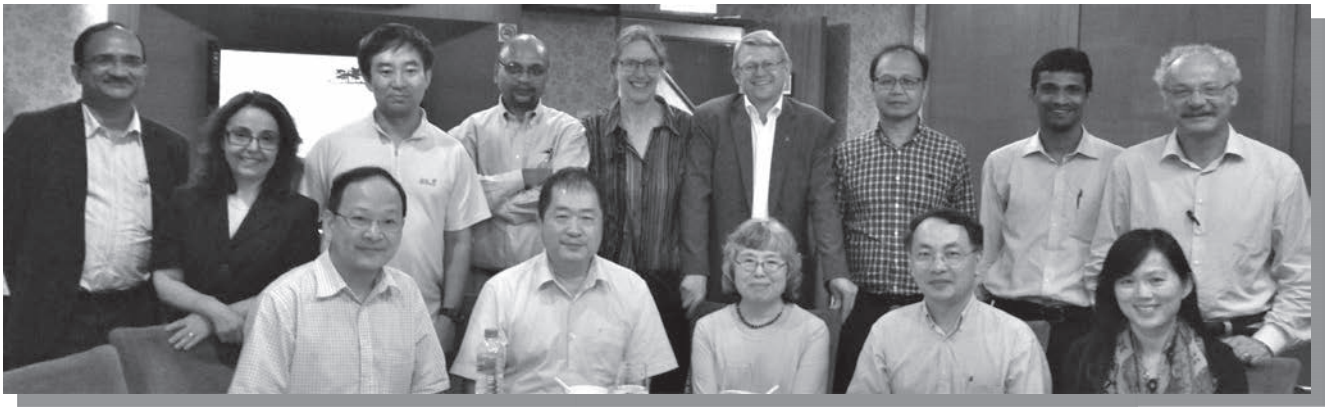
The **MQ-1** at Nanyang Technological University (NTU) were attended by 4 DLs: Prof. Zeynep Celik-Butler (UT-Arlington), topic: *"A Comprehensive Physics-Based, Measurement-Driven Random Telegraph Signals Model for MOS System;"* Dr. Simon Deleonibus (LETI), topic: *"Towards Zero Intrinsic Variability and Zero Power Future Full 3D Micro/nano-electronics;"* Prof. Anisul Haque (East West University), topic: *"Extraction of Interface Trap Densities in High-Mobility Semiconductor MOSFETs;"* and Prof. Ramgopal Rao (IIT-Bombay), topic: *"Polymer MEMS: Opportunities and Challenges."*

The **MQ-2** at National University of Singapore (NUS) had 4 DLs: Prof. Albert Chin (National Chiao Tung University), topic: *"Ultra-low power and Energy Efficient Green Electronic Devices;"* Prof. Mitiko Miura-Mattausch (Hiroshima University), topic: *"Physics of High Voltage Devices and Their Applications;"* Prof. Mikael Ostling (KTH), topic: *"Very High Voltage SiC Power Switches Energy Efficient Integrated SiC Drive Electronics;"* and Prof. Bin Yu (SUNY-Albany), topic: *"Nanostructure-based Future Devices."*

The **MQ-3** at Singapore University of Technology and Design (SUTD) had 3 DLs participating. Prof. Mansun Chan (Hong Kong University of Science and Technology), topic: *"A New Paradigm for Circuit Reliability Simulation with Model Embedded Aging Modules;"* Prof. Juin Liou (University of Central Florida), topic: *"Compact Modeling of Electrostatic Discharge (ESD) Induced Failure in Semiconductor Devices;"* and Prof. Ming Liu (Institute of Microelectronics, Chinese Academy of Sciences), topic: *"Reliability Issues of Oxide Electrolyte Based CBRAM."*

All these MQs were attended by local university students and EDS members.

At the end of the respective MQs, the DLs were presented a token of appreciation by the hosts on behalf of the chapter, followed by a dinner for the participating DLs. This was followed by two other WIMNACT programs by two groups of DLs at Bandung, Indonesia and Perth, Australia on June 8, 2015. These jointly organized events demonstrated best sharing of resources for the MQ funds and DLs' travel for serving our chapters.



The DLs and local hosts participating in the WIMNACT-47 in Singapore

WIMNACT-48 IEEE EDS Mini-Colloquium at Bandung, Indonesia

By Ihsan Ariadi

The 48th IEEE Workshop and Colloquium on EDS Mini-Nanometer CMOS Technology (WIMNACT-48) was successfully held June 8, 2015, at the central library of Institut Teknologi Bandung (ITB), Bandung Indonesia, as a joint collaboration between The School of Electrical Engineering and Informatics, ITB and the IEEE Electron Devices Society, supported by ITB Microelectronics Center. About 50 participants from academic institutions including students and professors participated in this event. The presence of four IEEE Distinguished Lecturers from various fields of science seemed to be a strong attraction.

Prof. Juin J. Liou of the University of Central Florida gave the first talk on the latest developments in the technology of protection against electrostatic discharge (ESD) in low voltage RF IC applications. Prof. V. Ramgopal Rao of IIT Bombay, delivered an interesting perspective on the Opportunities and Challenges of the polymer MEMS. Polymers enable fabrication of MEMS/NEMS devices with superior electro-mechanical characteristics as Compared to the traditional silicon MEMS, including in a low-cost sensor applications. Prof. Bin Yu of the State University of New York, gave a talk on the future of graphene-based electronics. Graphene and its derivative material systems have received significant amount of research interests from both academia and industry. In the last session, Prof. Basuki Rahmatul Alam of Institute Teknologi Bandung gave a talk on the perspective of teaching in Indonesia entitled, *"Teaching Factory as part of integrated education concept in preparing manpower for Microelectronics Industry in Indonesia."*

The DLs, the local organizer and participants of WIMNACT-48 at Institut Teknologi Bandung, Bandung, Indonesia

WIMNACT-49 EDS Mini-Colloquium at Perth

By Adam Osseiran

The Joint 49th Workshop and IEEE EDS Mini-colloquium (MQ) on NAnometer CMOS Technology (WIMNACT) was successfully held June 8, 2015, in Perth. It was co-organized by the joint EDS/SSCS/IPS Chapter of the Western Australia (WA) Section and the Microelectronic Research Group (MRG) of the University of Western Australia (UWA). Three Distinguished Lecturers (DLs) participated in the workshop as well as a number of specialists from the MRG group at UWA. The three DLs were Prof. Mansun Chan of the Hong Kong University of Science and Technology, Prof. Xing Zhou of the Nanyang Technological University in Singapore (NTU), and Prof. Lorenzo Faraone of the University of Western Australia (UWA).

The MQ talks covered a wide range of topics including: "Compact Modeling Beyond Device Physics" by DL Prof. Mansun Chan, "*Optical MEMS for multi-spectral chem/bio sensing and imaging: from NIR to LWIR*" by DL Prof. Lorenzo Faraone, "*Combining silicon photonics and MEMS for robust, ultra-sensitive chemical sensors*" by Dr. Gino Putrino of MRG, "*Unified platform for EM wave manipulation and imaging: from UV to THz*" by Dr. Dilusha Silva

The 49th WIMNACT in Perth on June 8, 2015. (front row from left to right) Prof. Adam Osseiran, Prof. Lorenzo Faraone, Prof. Xing Zhou, Prof. Mansun Chan, Prof. Brett Nener, Prof. Gia Parish, and Dr. Jarek Antoszewski

of MRG, "*AlGaN/GaN transistor based sensors*" by Prof. Gia Parish of MRG, "*A Unified Compact Model for Generic HEMTs*" by DL Prof. Xing Zhou, "*Mobility spectrum analysis of carrier transport at insulator/semiconductor interfaces*" by Dr. Gilberto Umana-Membreno of MRG, "*GaSb alternative substrates for MBE growth of HgCdTe*" by Dr. Wen Lei of MRG and finally "*HgCdTe-based IR sensor technology at UWA*" by Dr. Jarek Antoszewski of MRG.

The Perth MQ was hosted by the University of Western Australia (UWA) and was attended by 32 faculty and students. The joint WIMNACT was financially supported by the EDS with co-sponsorships from UWA as well as the WA IEEE Section and was a very successful event for promoting ED-related activities. The joint ED chapter in Western Australia has been very active in electron-device and photonics-related activities, and the visit by the EDS delegation has brought scholarly exchange among professional colleagues and students. This should help promote more ED-related activities in Australia.

2015 IEEE International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA)

The IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2015) was held at the Lakeshore Hotel, Hsinchu Science Park, Taiwan, from June 29 to July 2, 2015. It was the 26th year of IPFA and it has been one of the major conferences in the reliability and failure analysis of devices and integrated circuits. Organized by the IEEE ED Taipei Chapter and the IEEE Singapore Reliability/CPMT/ED Chapter, the Symposium is technically co-sponsored by the IEEE Electron Devices and IEEE Reliability Societies. This is the second time that the symposium was held in Taiwan at the Lakeshore Hotel, which is next to the very first Science Park, the well-known "Taiwan Silicon Valley." Also nearby, the famous Green Grass Lake, once one of the top eight scenic attractions that has been recently renovated and holds good memories for the people of Taiwan.

The IPFA 2015 includes a one-day tutorial, a three-day technical paper presentation, and concurrently with exhibits from worldwide vendors. A one-day tutorial, scheduled for Monday, June 29th covers four topics in two parallel sessions. This brings up an excellent opportunity for experienced engineers, scholars, professors, and students, to broaden their technical knowledge in both reliability and failure analysis techniques. Vendor exhibits presented state-of-the-art advanced techniques, equipment on failure analysis, testing and measurement, etc., which were held in parallel with the technical sessions.

In this symposium there were more than 185 submissions from 15 countries, in which 60 papers were selected for oral presentations, and 77 for poster presentations. We also had 15 excellent invited talks which received good feedback, along with two outstanding exchange papers contributed from ISTFA 2014 and ESREF 2014, respectively. More than 300 participants attended the symposium with 28 equipment vendors showing their equipment and facilities concurrently with the technical paper sessions.

A one-day tutorial session that preceded the 3-day conference program featured comprehensive technical reviews on a wide range of topics: (1) Advanced Technology Scaling and Reliability Challenges (Dr. Yung-Huei Lee, TSMC); (2) Dynamic Fault Isolation Techniques and Case Studies (Dr. Michael Bruce, Consultant, USA); (3) Electrostatic Discharge (ESD) Protection of Low-Voltage RF Integrated Circuits (Prof. Juin J. Liou, University of Central Florida, USA); and (4) Applications of Materials and Failure Analysis Techniques in Semiconductor Industries (Dr. Chih Hsun Chu, Materials Analysis Technology Inc., Taiwan).

The conference had two distinguished keynote speakers for the plenary session. Dr. Antony S. Oates, TSMC, presented a talk on *"Reliability and Technology Scaling Beyond the 10nm Node."* Reliability will be a key enabler for future generation Si process technologies. He addressed several important issues of the reliability, such as the development of high quality semiconductor/dielectric interfaces and gate dielectric stacks; back-end dielectrics that eliminate the inherent vulnerability of porous materials; Soft-errors can be expected to be exacerbated with the introduction of high mobility channels, requiring the development of circuit level mitigation techniques.

Dr. Xin Wu of Xilinx, addressed on *"3D-IC FPGA: KGD, DFT and Build-in FA capabilities."* On the development of 3D-IC products, cost is one of the top concerns. Practical experiences on the study of FPGA technology development and manufacturing were presented. Within cost elements, known-good-die (KGD) and 3D-IC integration yield are among a few biggest impacting factors. In order to achieve high 3D-IC integration yield, build-in self-repairing, design-for-testing (DFT), diagnostic, and failure analysis (FA) capabilities, are very important elements for a successful development of 3D-IC FPGA.

The symposium also featured a selection of Best posters and Best papers. Best papers are:

1) Two best papers in FA (Failure Analysis) and Reliability respectively:
   (*Failure Analysis*) Fault Isolation Using Electrically-enhanced LADA (EeLADA), by Szu Huat Goh et al., *GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore;*
   (*Reliability*) UTB GeOI 6T SRAM Cell and Sense Amplifier Considering BTI Reliability, by Vita Pi-Ho Hu et al., National Chiao Tung University, Taiwan
2) Two best posters:
   (*Failure Analysis*) Static Fault Localization on Memory Failures using Photon Emission Microscopy, by N. Dayanand et al., *GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore;*
   (*Reliability*) A Comparison Study on the Al-based Interfacial Layers for Ge MIS Devices, by Yi-Gin Yang et al., National Chiao Tung University, Taiwan

The ED Taipei Chapter also promoted IEEE membership by selecting ten students from among the symposium participants and awarded them each one-year complimentary membership. Certainly this was a good move to encourage more young professionals to join the IEEE as well as promoting the IEEE activities.

2016 IPFA will be back in Singapore, July 4-8 at Marina Bay Sands. For more details, please visit: http://ieee.org/ipfa

Steve S. Chung, 2015 IPFA
General Chair
Vinod Narang, 2015 IPFA
General Co-Chair

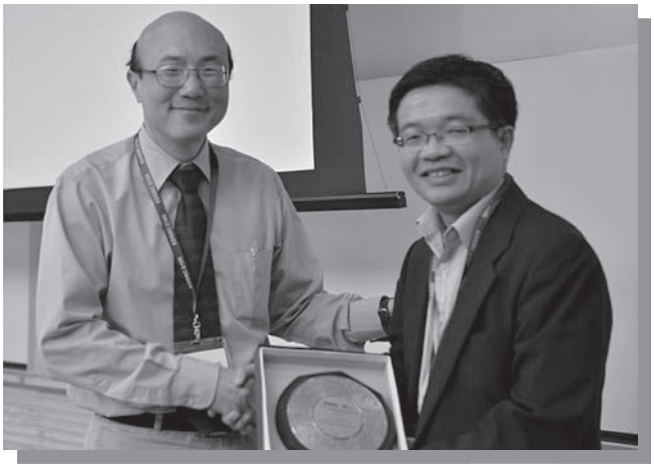
2015 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC'2015)

By Chuan Seng Tan (on behalf of the EDSSC'2015 Organizing Committee)

The 2015 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC'2015, www.edssc2015.org) was successfully held in Singapore, June 1–4, 2015. The conference was sponsored by the IEEE Electron Devices Society (EDS), IEEE Singapore Section Rel/CPMT/ED Chapter, and IEEE ED/SSC Hong Kong Section Chapter. It was also supported by the IEEE SSCS Singapore Chapter. The EDSSC'2015 was a four-day program and included keynote and invited speeches, oral and poster sessions, as well as tutorials covering a broad range of topics in electron devices, circuits and systems. The three keynotes were given by Prof. Eugene Fitzgerald of MIT, Prof. Thomas Lee of Stanford University, and Prof. Dim-Lee Kwong of IME, A*STAR. Altogether, there were 29 invited talks by experts in the fields. Out of a total of 270 regular submissions from Asia, Europe and US, the 56-member Technical Program Committee (TPC) deliberated and accepted 130 oral papers and 84 poster papers. Four students were awarded the Best Student Poster Awards. The four-day event went well with more than 200 participants and 8 exhibitors. Next year's conference will be held in Hong Kong.

Prof. Xing Zhou, General Chair, presented a token of appreciation to Prof. Eugene Fitzgerald (right) after the keynote speech

Prof. Kin-Leong Pey, General Co-Chair, presented a token of appreciation to Prof. Dim-Lee Kwong (left) after the keynote speech



Prof. Chuan Seng Tan, TPC Chair, presented a token of appreciation to Prof. Thomas Lee (left) after the keynote speech

The steering committee and organizing committee of EDSSC 2015 at the Marina Bay Sands, Singapore

2015 IEEE International Vacuum Electronics Conference – IVEC2015

By Jinjun Feng, Technical Program Chair, IVEC2015

The 16th IEEE International Vacuum Electronics Conference (IVEC2015) was held in Beijing China at the elegant Beijing International Convention Center (BICC) April 27–29, 2015. This is the first time IVEC was held in China and the fourth in Asia after Seoul, Korea (IVEC2003), Kitakyushu, Japan (IVEC2007) and Bangalore, India (IVEC2011). IVEC2015 was organized jointly by the Beijing Vacuum Electronics Research Institute (BVERI), IEEE Beijing Section, University of Electronics Science and Technology of China (UESTC), and National Key Laboratory of Science and Technology on Vacuum Electronics (NKLST-VE).

IVEC2015 attracted over 440 scientists, engineers and students from 13 countries and regions including USA, France, Russia, UK, Germany, Korea, Japan, Brazil, Singapore and China, etc. There were a total of 374 papers accepted in research areas covering vacuum electron sources, vacuum microelectronics, microwave electronics, vacuum electronic devices, etc. There was one plenary session, 28 regular oral sessions, and 5 poster sessions. For the first time in IVEC history, a fully independent session on metamaterials was included.

In the plenary session, five well-known experts in vacuum electronics and related fields gave invited presentations. First, Prof. Shenggang Liu from the UESTC reported on *"Recent Development of Vacuum Electronics on Terahertz and Light Radiation."* Prof. Neville Luhmann from University of California at Davis reported on *"Advances in Microfabricated Millimeter Wave and THz Vacuum Electronic Devices and Their Applications,"* followed by Prof. Kwo-Ray Chu from National Taiwan University with *"Some Recent Progresses on Electron Cyclotron Maser Research."* Prof. Jiangang Li from the Chinese Academy of Sciences spoke on *"Microwave Application in Tokamak EAST and Future Needs for Next-Step fusion Reactor,"* and Chuanxiang Tang from Tsinghua University, China, reported on "An Overview of the Links Between Vacuum Electronics and Particle Accelerators." They introduced the latest international developments on terahertz vacuum radiation, gyrotrons, ITER (International Thermonuclear Experimental Reactor), and accelerator technology, respectively.

The 154 papers presented in the 28 oral sessions included topics such as field emission and FE devices, magnetrons, device analysis and simulation, helix traveling wave tubes, MBK/EIKs, gyrodevices (including amplifiers, oscillators, components and quasi-optical technology), W-band traveling wave tubes, thermionic cathodes (fundamental technology and applications), 220 GHz traveling wave tubes, high power microwave and relativistic devices, millimeter wave traveling wave tubes, materials and technology, metamaterials, systems and applications, terahertz (theory and devices), space traveling wave tubes, klystrons and IOTs. The other 220 papers were presented in the 5 poster sessions.

The IVEC2015 Plenary Session Audience

The BVERI reception banquet was held the evening of April 28th. Over 100 staff and graduate students from BVERI made a brilliant performance at the banquet including Peking Opera, ethnic songs and dances, Chinese calligraphy, hip-hop and pop songs. During the banquet, the IVEC2015 Best Student Paper Award was announced. Dr. Jinjun Feng, currently Chair of IEEE Beijing Section, introduced the IEEE Beijing Section, and gave the 8 best student paper candidates each an engraved glass souvenir marking the 30th anniversary of the establishment of IEEE Beijing Section. He encouraged them to contribute to the IEEE and expressed optimism they are the future of vacuum electronics. The Student Paper Award Committee Chairman, Prof. Paoloni Claudio from Lancaster University, UK, introduced the selection process, and Co-Chairman Prof. Yubin Gong from UESTC announced the results. This year Geoffrey Greening from the University of Michigan was the winner of the Best Student Paper Award for his paper entitled *"Experimental Microwave Power Extraction in the Multi-frequency Recirculating Planar Magnetron."* Further information on IVEC2015

can be found at http://cie-china.org/ivec2015/.

Finally, we are pleased to announce that IVEC2016 will return to Monterey, California, USA. The conference will be held at the Marriott Conference Center, April 19–21, 2016. Dr. David Whaley from L-3 Communications as General Chair assisted by Dr. Monica Blank from Communications and Power Industries will be Technical Program Chair.

Dr. Kevin Felch

Dr. Richard True

John R. Pierce Award for Excellence in Vacuum Electronics

This year, Dr. Kevin Felch from Communications and Power Industries received the prestigious John R. Pierce Award for Excellence in Vacuum Electronics. This is the highest award in the field of Vacuum Electronics. The award was presented in the Plenary Session of IVEC2015 by Dr. Richard True, Chair of IEEE EDS Vacuum Electronics Technical Committee. Dr. Felch received an engraved plaque with the *citation "for pioneering research and leadership in the development of gyrotrons for fusion energy sciences and national defense"* and a check for $2000. Dr. Felch delivered a highly enjoyable speech following entitled *"A Gyrotron Journey"* that traced his life and life experiences from childhood to the present. Interwoven throughout the speech were his numerous technical achievements in the development of super high power gyrotrons and other fast wave devices.

For readers who are interested in further information about Dr. Felch and other winners of the John R. Pierce Award see http://vacuumelectronics.org/awardpage.html.

Chapters in Community Activities

Nepal Earthquake (April 2015) and ED Nepal Chapter

By Raju Khanal, ED Nepal Chapter

Nepal, a beautiful mountainous country, was hit by a disastrous earthquake of magnitude 7.8 (on the Richter Scale), on April 25, 2015. Thousands of houses were destroyed across the country, with entire villages flattened, especially those near the epicenter. In addition, the earthquake triggered avalanches in various parts of the country which, in some cases, swept whole villages and also a few tourist camps up high in the Himalayas. The disaster killed nearly 9,000 people, many more injured, destroyed many homes, millions of people were affected and various parts of the country were

Visit of affected village site by IEEE EDS members

Earth quake destroyed schools in Nepal (photo credit: UNICEF)

cut-off due to damaged roads and other infrastructure. Members of the IEEE EDS Nepal Chapter actively took part in various volunteer activities immediately after the earthquake. As the aftershocks continued for a prolonged period of time and of high magnitude (more than 300 aftershocks in one month) it was not possible for the members to come together for any coordinated activities. The members were active in their respective areas where they provided helping hands for cleaning debris, collecting necessary foods, tents and cloths for displaced people and also in raising funds.

The moral of local members was boosted by a team of IEEE and EDS members from India (Mr. Amarnath Raja, Mr. Harish Mysore, Mr. Jaideep Bansal and Mr. M. C. Jayakrishnan), who visited Nepal right after the earthquake to access the situation and to discuss about the help needed or that can be delivered. Their visit took place when the aftershocks of magnitude of about 4.5 were still continuing once or twice a day. After initial interactions with various local members and visiting a few nearby sites, the team had formal discussions on identifying the scope and location of interventions. On the third day, the visiting team accompanied by local members went to a village near the Upper Tamakoshi Hydropower site, which was accessible by a 7 hour car ride from Kathmandu and then a 3 hour trek. The village was off-grid after the earthquake and most of the houses have fallen and the first priority in the minds of the villagers is civil reconstruction. The visiting team agreed to prepare a proposal to concretize the plan of action and the resource requirements, expected partners and funding support and it worked well. Local members coordinated by Mr. Bigyan P. Shrestha, who is also involved in the Hydropower project are helping in the civil works and the 200 Solar Lanterns received from the IEEE Kerala Section have already been distributed.

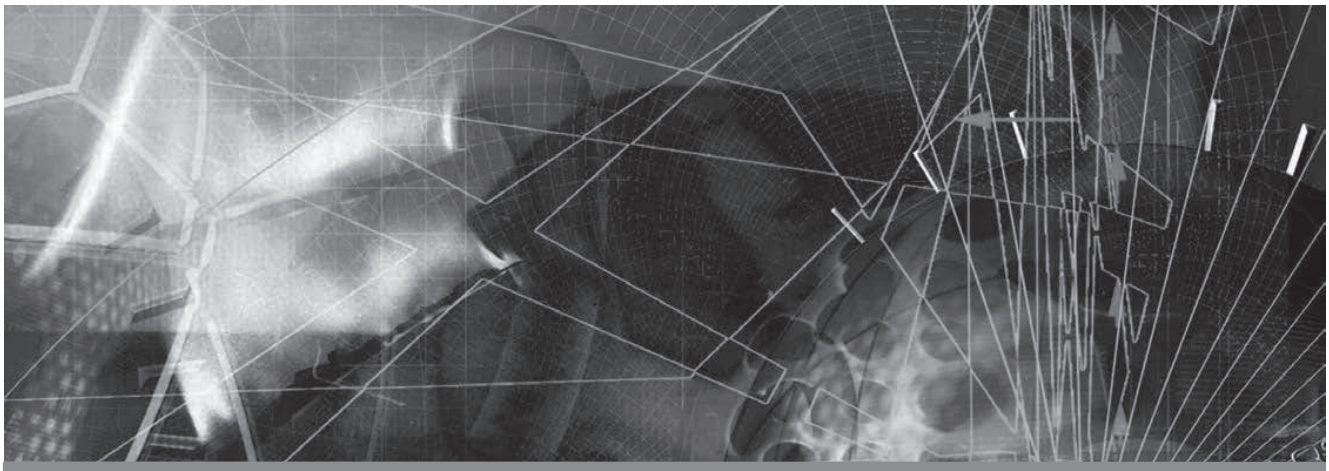
The Education sector especially the schools, were also badly hit by the earthquake. Almost all the schools in the affected area are damaged and only about 10% of the schools were in a condition to be used after minor repair. The Colleges / Universities in the area were also affected and shut down for more than a month. The academic institutions are now all running but lack in infrastructure and it will take a long time before they are fully renovated and operational. In most cases, they are running in temporary sheds. As most of the IEEE EDS members are affiliated to academic institutions they are active from their level to reinstate infrastructure and other facilities in their institutions. However, because of the large scale and wide spread destruction of buildings, laboratory facilities and other amenities the restoration process needs to be undertaken for a prolonged period and requires support from various sectors. The members of IEEE EDS Nepal Chapter have been contributing from their level and are willing to devote their time and effort in the process of rebuilding.

Singapore Chapter Members at Children's Home and Gracehaven

By Chee Lip Gan

The Singapore ED/REL/CPMT chapter organized a social, good-hearted event with a dinner and movie screening of "Minions" on June 20, 2015, for 80 children and their guardians coming from Chen Su Lan Methodist Children[1]s Home and Gracehaven. A total of 165 participants attended the event including Chapter committee members and their families. The dinner was arranged for everyone at the Pepper Steakhouse & Bistro before the movie screening. Chapter members had a wonderful evening with all the children and their guardians of the Children's Home and members of Gracehaven, who were so delighted and touched by the generosity, approach and involvement of the Chapter members. Based on the excellent feedback received, the Chapter plans to organize another similar event later this year.

Singapore Chapter members before the movie screening



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IEEE

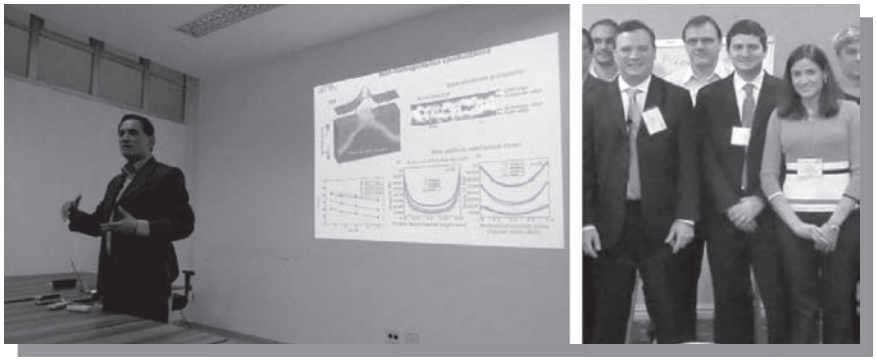
Regional News

USA, Canada & Latin America (Regions 1-6, 7 & 9)

ED Montreal Chapter

Prof. Karim S. Karim of the University of Waterloo was invited by the Electron Devices Society Montreal Chapter to deliver an IEEE EDS Distinguished Lecture, titled *"Ultra-high resolution amorphous selenium-CMOS hybrid X-ray imagers for bioengineering applications,"* at Concordia University, Montreal, Canada, on July 15, 2015. The talk highlighted current areas in bioengineering and life sciences where ultra-high resolution X-ray imagers can find new application. X-ray imaging is a valuable alternative for *in vivo* imaging of small animals such as mice in genomics and cancer research. Active discussion was conducted after his talk.

~Karim S. Karim, Editor



Prof. Edmundo Gutierrez during his lecture (left) and (right) Prof. Joao Martino, Prof. Victor Sonnenberg, Ms. Marcio Martino and Profa. Paula Agopian

Prof. Cor Claeys at the University of Sao Paulo, Brazil

ED South-Brazil Chapter

University of Sao Paulo, Brazil

–by Joao Antonio Martino, Chapter Chair, Paula Agopian, Vice-Chair

The ED South Brazil Chapter organized two Distinguished Lecturer Presentations (DLP) in April 2015, at Polytechnic School of University of Sao Paulo, Brazil.

The first presentation on April 7th, given by Prof. Dr. Edmundo Gutierrez from National Institute for Astrophysics, Optics and Electronics INAOE, México, was entitled, "Thermo-magnetic effects in nano scaled FET's: characterization, modelling, and simulation." After his presentation, he had an opportunity to visit the Laboratory of Integrated System of University of Sao Paulo, followed by a technical meeting with Prof. Joao Martino's research group.

Karim S. Karim (standing right) at the ED Montreal Chapter's Distinguished Lecture event

The second DLP was on April 17th, and given by Prof. Dr. Cor Claeys, from imec/Belgium, entitled *"Internet of Things."* After the presentation, Prof. Cor Claeys had a meeting with Prof. Joao Martino and Profa. Paula Agopian from University of Sao Paulo, concerning the long-term cooperation with imec of around

25 years on SOI MOSFET, FinFET and more recently on Tunnel-FET devices.

In each DLP, we had around 30 people including IEEE ED members, undergraduate and graduate students of several universities in the region.

ED Student Branch Chapter at FEI

—by Genaro Mariniello da Silva, Chapter Chair, Marcelo Pavanello and Michelly de Souza, Chapter Advisors

At SEMINATEC 2015 (left to right): Prof. Joao Martino, Prof. Edmundo Gutierrez, Prof. Marcelo Pavanello, Prof. Nilton Morimoto, Prof. Antonio Petraglia, and Prof. Edval Santos

At SEMINATEC 2015 (left to right): Prof. Rodrigo Doria, Prof. Salvador Gimenez, Prof. Gilson Wirth, Prof. Marcelo Pavanello, Prof. Renato Giacomini, Prof. Michelly de Souza, and Dr. Renan Trevisoli

The X Workshop on Semiconductors and Micro & Nano Technology – SEMINATEC 2015 was held at the Sao Bernardo do Campo *campus* of Centro Universitario da FEI, Brazil, April 9th and 10th. SEMINATEC 2015 has been a continuation of previous workshops, all focused on technology trends in the areas of micro and nanotecnology.

The SEMINATEC was organized by Centro Universitario da FEI, and promoted by the IEEE FEI ED Student Branch Chapter, the IEEE ED South Brazil Chapter, the IEEE UNICAMP ED Student Branch Chapter, the IEEE SSCS Chapter of the South Brazil Session, the Brazilian Microelectronics Society, and the NAMITEC Science & Technology National Institute.

For this edition of the Workshop six Invited Speakers participated, covering a variety of topics in the Micro & Nano Technology fields: Prof. Edmundo A. Gutiérrez (IEEE EDS Distinguished Lecturer), from INAOE, Mexico, with the presentation *"Thermo-magnetic effects in nano scaled FET's: characterization, modelling, and simulation;"* Prof. Edval Santos (IEEE EDS Distinguished Lecturer), from Federal University of Pernambuco (UFPE), Brazil, with the presentation *"Smart sensor technology for niche applications;"* Prof. Antonio Petraglia, from Federal University of Rio de Janeiro (UFRJ), Brazil, with the presentation *"On-chip capacitance ratio measurement using a switched-capacitor filter;"* Prof. Gustavo Dalpian, from Federal University of ABC (UFABC), Brazil, with the presentation *"Theory of resistive switching in Memristors;"* Eng. Raphael Mendes Motta, from Tektronix, Brazil, with the presentation *"Semiconductor Analysis from Attoampere to Kilovolts;"* and Prof. Gilson Inácio Wirth, from Federal University of Rio Grande do Sul (UFRGS), Brazil, with the presentation *"Reliability of MOS Devices and Circuits."*

Also a presentation about the last achievements of the project *"Science & Technology National Institute on Micro and Nanoelectronic Systems – NAMITEC,"* a nation-wide project involving research groups from 24 institutions working in Micro & Nanotechnologies in Brazil has been given by Prof. Nilton Morimoto, from University of Sao Paulo (USP).

In its two days a total of 224 people registered for the Workshop, including undergraduate and graduate students from several universities in the region, such as FEI, USP, UNICAMP, UFABC, among others, as well as from companies and research centers, such as Centro de Tecnologia da Informação Renato Archer, Cistek, Tektronix, Atech and LSITEC.

Following the previous workshops, additionally to the Invited Speakers presentations, 29 papers were selected by the Program Committee to be presented at the Workshop in a Cocktail and Poster Session as well as to be included in the Workshop Proceedings.

The funding for the Workshop was given by the Brazilian National Council of Science and Technology (CNPq), as recognition of its relevance as well as the relevance of this field to the country.

~Joao Antonio Martino, Editor

Europe, Middle East & Africa (Region 8)

ED Poland – 3rd Training Course on Compact Modeling

–by Daniel Tomaszewski, Editor and Wladek Grabiński

A 3rd Training Course on Compact Modeling (TCCM) was held in Torun (Poland), June 24, 2015. It followed the previous two TCCM issues (2010, 2012), which were organized within a FP7 project "Compact Modeling Network" (COMON). The 3rd TCCM was organized within IEEE EDS Distinguished Lecturer Mini-Colloquia Program (http://eds.ieee.org/lectures.html?eid=136). The event was additionally supported by Instytut Technologii Elektronowej, Warsaw, and by Lodz University of Technology, Department of Microelectronics and Computer Science as a technical promotor.

The course was addressed to IC Process, Characterization, Modeling, and Design engineers who actively used compact modeling of semiconductor devices. During the course six lectures were presented:

1) "*Weaknesses and Corrections of the Classical Theory of Photoelectric Phenomena in the MOS System,*" Prof. H. Przewlocki (IEEE DL),
2) "*Compact Modeling of Junction Failure in Semiconductor Devices Subject to Electrostatic Discharge Stresses,*" Prof. J. J. Liou (IEEE DL),
3) "*A Unified Approach to Compact Device Modelling with the Open Source Packages Qucs/ADMS and MAPP/Octave,*" Prof. M. Brinson (IET Member),
4) "*Physically-Based Compact Modeling of GaN HEMT*", Prof. B. Iniguez (IEEE DL),
5) "*Verilog-A Compact Model Standardization,*" Dr. W. Grabinski (IEEE DL),
6) "Compact Modeling and Statistical Modeling for Parametric Yield Improvement," Dr. D. Tomaszewski (EDS Member).

The talks covered different subdomains of semiconductor device compact modeling, including device physics, compact modeling, its implementation, standardization, and application for design for manufacturability. The topics triggered interesting discussions between attendees and speakers.

The meeting attended by representative of industry (Infineon, Bosch) and academia (AGH Krakow, University of Cambridge) was held in a very good, informal atmosphere, which facilitated the technical discussions.

Joint Meeting of ED and SSC IEEE Poland

On June 27, 2015, Toruń, Poland, a joint meeting of Poland Section of IEEE Electron Devices Chapter and Solid-State Circuits Society Chapter took place. The meeting began with a presentation by Prof. Paweł Gryboś and Dr. Piotr Kmon from AGH University of Science and Technology entitled, "*Designing Ultra-Low-Voltage Analog Circuits.*" Also, the ED Chapter Poland Section election for chapter chairs was held in July.

Prof. Gryboś and Dr. Kmon's presentation on June 27th

Poland Mini-Colloquium lecturers and organizers

22nd International Conference "Mixed Design of Integrated Circuits and Systems" – MIXDES 2015

On June 25–27, 2015, Toruń, Poland, the annual International Conference MIXDES 2015 was held. The event was organized by the Lodz University of Technology together with the Warsaw University of Technology in cooperation with Military Institute of Aviation Medicine and ROS3D Consortium. The conference was co-sponsored by Poland Section IEEE ED & CAS Societies, Polish Academy of Sciences, Committee of Electronics and Telecommunication, Section of Microelectronics and Sections of Signals and Electronic Circuits and Systems and Commission of Electronics and Photonics of Polish National Committee of International Union of Radio Science – URSI.

22nd International Conference "Mixed Design of Integrated Circuits and Systems" – MIXDES 2015 was a successful scientific meeting. This year we met together in Toruń – a medieval metropolis in the center of Poland – especially known as a home town of Nicolaus Copernicus. The MIXDES 2015 three-day program included invited speeches, as well as 116 oral and poster presentations reviewed and selected from all submissions from 21 countries.

In addition to the regular program, there were seven invited speakers including Prof. Juin J. Liou who received the IEEE Electron Devices Society Education Award in 2014 for promoting and inspiring global education and learning in the field of electron devices:

- *Challenges in Design-oriented Modeling in Biology*
  Prof. Christophe Lallement (University of Strasbourg, France)
- *Energy Efficency Optimization for Digital Applications in 28 nm UTBB FDSOI Technology*
  Prof. Amara Amara (ISEP, France)
- *Formal Methods – Support or Scientific Decoration in Software Development?*
  Prof. Tomasz Szmuc (AGH University of Science and Technology, Poland)
- *Prospect and Outlook of Electrostatic Discharge (ESD) Protection in Emerging Technologies*
  Prof. Juin J. Liou (University of Central Florida, USA)
- *Silicon PhotoMultipliers: Introducing the Digital Age in Low Light Detection*
  Prof. Massimo Caccia (Universita' dell'Insubria, Italy)
- *Single-Event Effects in Advanced CMOS Technologies – Analysis and Mitigation*
  Dr. Marek Turowski (Robust Chip Inc., USA)
- *The Future is MEMS Design Considerations of Microelectromechanical Systems at Bosch*
  Dr. Mike Schwarz (Robert Bosch GmbH, Germany)

The sessions also included presentations in the frame of three special sessions:

- *Biomedical Measurement Technologies*
  organized by Dr. Olaf Truszczyński, Prof. Marek Prost (Military Institute of Aviation Medicine, Poland) and Prof. Witold Pleskacz (Warsaw University of Technology, Poland)
- *Issues of Stereoscopic 3D Technologies and Image Acquisition in Current R&D*
  organized by ROS3D Consortium
- *Open Source Compact/SPICE Modeling*
  organized by Dr. Daniel Tomaszewski (Institute of Electron Technology, Poland) and Dr. Władysław Grabiński (GMC Suisse, Switzerland)

The authors of selected papers received the *Best Paper Award* diplomas and the Polish Section of IEEE ED Chapter presented the best student paper award to Sylvain Noblecourt for the paper entitled "*An Improved Junction Termination Design Using Deep Trenches for Superjunction Power Devices.*"

The next MIXDES 2016 Conference will take place in Lodz. The Preliminary Call for Papers is available at http://www.mixdes.org/downloads/call2016.pdf. More information about the past and next MIXDES Conferences can be found at http://www.mixdes.org.

~Mariusz Orlikowski, Editor

Attendees of the International Conference MIXDES 2015

ED Dublin/PHO Ireland
—by Patrick McNally

The joint chapter of the Dublin Electron Devices and the Ireland Photonics Societies hosted Professor Simon Deleonibus of CEA LETI, Grenoble France, who delivered an IEEE Distinguished Lecture entitled *"More More and Moore than More meeting for 3D"*. Prof. Deleonibus is Chief Scientist at CEA LETI and is one of the world's foremost researchers in semiconductor nanodevices. He is a Fellow of the IEEE and of the Electrochemical Society and is Visiting Professor at the Tokyo Institute of Technology. He is also a participant in defining the International Technology Roadmap for Semiconductors, serves on the IEEE Electron Devices Society Board of Governors and was a former Editor of the IEEE Transactions on Electron Devices.

His lecture was hosted by the Rince Institute in Dublin City University on June 26th 2015 and an audience of over fifty attendees heard Prof. Deleonibus discuss how new design and functional architectures mixing logic and memory devices can be used to increase device performance and complexity but at the same time reduce power consumption. He also discussed how non-CMOS technologies (e.g. MEMS, sensors, etc.) can be integrated to provide for these new functionalities.

His lecture was video linked live to the Tyndall National Institute in Cork, Ireland, and the large audience was appreciative of a stimulating and fascinating glance into the future of nanoelectronics.

Professor Simon Deleonibus (CEA LETI, Grenoble, France) speaking at the Rince Institute in Dublin City University, Ireland

~Jonathan Terry, Editor

The 38th International Semiconductor Conference (CAS 2015)

The conference is scheduled to be held in Sinaia, Romania, October 12–14, 2015. The CAS conferences have been organized since 1978. They have become international events since 1991. Since 1995 they have been sponsored by IEEE Electron Devices Society. In the last decade, the Conference profile has been extended from semiconductor devices physics and technology (including materials and microelectronics) towards micro- and nanotechnologies. Recently the Conference topics are as follows:

- Nanoscience and Nanoengineering
- Micro- and nanophotonics and Optoelectronics
- Microwave and Millimeter Wave Circuits and Systems
- Microsensors and Microsystems
- Modelling
- Semiconductor Devices
- Integrated Circuits
- Physics of Materials

Since 1997 the CAS conferences have been organized by the National Institute for Research and Development in Microtechnologies (IMT-Bucharest, www.imt.ro). IMT is supervised by the Romanian Ministry of Education and Scientific Research. IMT mission consists in research and development in micro-nano-bio-technologies, technology transfer, education and training, dissemination. The institute is oriented on a multidisciplinary research, integrating research, education and technology transfer, emerging as a regional centre. Between 2003 and 2015 IMT was involved in approximately 43 European projects (FP6, FP7 and related).

The CAS conference agenda includes a half-day plenary session, two and a half days of parallel technical sessions and a Student Paper Sessions. Best Student Paper Award is given every year by IEEE Romania Section EDS Chapter. Satellite events accompany the conference almost every year, including sessions organized by EC Projects, a thematic workshop "New trends in Automotive electronics and semiconductor", organized by Infineon Technology Romania, and "IEEE EDS Mini-Colloquium NADE – Nanoelectronic Devices – Present and Perspectives," organized by the IEEE EDS Romania Chapter. Recognized experts from academia and companies have been invited every year as speakers at the plenary sessions, e.g. Dr. M. C. Rocco, National Science Foundation USA, Dr. A. Wild, ENIAC Joint Undertaking Belgium, Prof. F. Udrea, Cambridge University UK, Prof. H. Hartnagel, Darmstadt University Germany, Prof. R. Sorrentino, University Perugia, Italy, Dr. D. Grützmacher, Forschungszentrum Jülich GmbH, Germany, and others.

For call for papers and further information regarding the conference, please visit the CAS website http://www.imt.ro/cas/. For additional information contact us at the email address: cas@imt.ro.

CAS General Chairman
Prof. Dan Dascalu (dan.dascalu@imt.ro)
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~Daniel Tomaszewski, Editor

Asia & Pacific (Region 10)

ED Taipei
–by Steve Chung

The ED Taipei Chapter held two invited talks in the second quarter of

ED Taipei Invited Talk (Left). April 30 – Prof. T. H. Hou (middle left, seminar host), Prof. Niha Mohapatra (middle right, speaker) (right) April 24 – Prof. Jason Woo (speaker)

2015. The first invited speaker, Prof. Jason Woo from the Electrical Engineering Department of UCLA, gave a talk entitled *"Low Power Transistor/Devices Physics."* He began with introducing the needs for low power requirement and examines several options, such as iMOS, tunneling FET, negative capacitance transistor, high mobility channel devices, etc. Then, he spent more time on delivering the concept of T-FET, several previous works on developing the steep subthreshold slope and enhanced Ion current of the transistor. He ended up with the possible and good solution of T-FET for low power applications. This talk was quite well-attended by more than 60 students, professors/researchers, as well as key leaders/engineers from TSME.

The second invited talk on April 24th with Prof. Nihar Mohapatra, from India Institute of Technology (IIT) Gandhinagar, was entitled, *"Anomalous Device Effects in HKMG MOS Transistors."* High-k/metal gate has been widely used for 45 nm and beyond generation. The new HKMG stack coupled with the smaller transistor dimensions give rise to many second order effects. In Prof. Mohapatra's talk, the anomalous device effects observed in HKMG MOS transistors was introduced. The effect of technology parameters like HfO_2 thickness, IL thickness, capping layer thickness and stress layer thickness on these anomalous device effects were presented. Finally some of the solutions to avoid these effects were provided. This talk was attended by more than 30 students and professors/researchers. A semiconductor facility tour was also arranged for our honored guest and some mutual discussion to promote student exchanges were also considered.

The chapter also organized an international symposium, IPFA 2015, held from June 29 to July 2, 2015, at the Lakeshore Hotel, Hsinchu Science Park, Taiwan. This is the second time this event was held in Taiwan, with its first move out of Singapore in 2004. The event consists of a one-day tutorial and a three-day technical paper presentation, in which more than 28 measurement/testing equipment exhibits were demonstrated concurrently. More than 300 participants attended the event. Next year, the symposium will be moved back to Singapore, with a paper submission deadline of February 5, 2016. The symposium dates are July 4–7, 2016, at Marina Bay Sand, Singapore. For more details, please visit the conference website: http://www.ieee.org/ipfa.

~Mansun Chan, Editor

ED Kansai

–by Michinori Nishihara

The ED Kansai Chapter held the 13th International Meeting for Future of Electron Devices, Kansai (2015IMFEDK) at Ryukoku University Kyoto Hall, Kyoto, Japan, June 4-5, 2015, with the theme of "New functional devices for the next generation."

The meeting attracted more than 110 attendees and was preceded by a tutorial seminar with two Distinguished Lecturers: 1) "Development history of blue light-emitting-diodes" by Dr. Masafumi Hashimoto, a retired researcher of Toyota Central R&D Labs., and, 2) "Fundamentals and Applications of Microwave Technology" by Prof. Toshio Ishizaki of Ryukoku University. The formal program began after the tutorial session with opening remarks by the general chair Prof. Yasuhisa Omura. The two day program featured a keynote titled "III-V/Ge MOSFETs and Tunneling FETs on Si platform for Low Power Logic Applications" by Prof. Shinichi Takagi of University of Tokyo. There also were three invited papers: 1) *"Nano-Channel InAlN/GaN Fin-HEMTs for Ultra- High-Speed Electronics"* by Prof. Subramaniam Arulkumaran of Nanyang Technological University; 2) *"Evolution of Nanoscale Silicon CMOS Technology for UltraLow Power Application"* by Dr. Takashi Matsukawa of AIST; 3) *"CMOS Circuits and Nanodevices for Spike Based Neural Computing"* by Prof. Takashi Morie of Kyushu Institute of Technology. In addition there were 17 papers in four regular technical sessions and a poster session with 33 posters with topics spreading out to Silicon, Compound, and Emerging Technologies. There were many students

2015 IMFEDK Awards Winners and Poster Session

discussing in front of their posters during the poster session.

At the end of the meeting the following awards were presented:

- IEEE EDS Kansai Chapter IMFEDK Best Paper Award to Hiroaki Fujihara of Kyoto University
- IEEE EDS Kansai Chapter IMFEDK Student Paper Award to the following five persons: Atsuya Suzuki (University of Fukui), Futo Hashimoto (Osaka University), Hongfei Lv (Kansai University), Ryota Kajimoto (Osaka Institute of Technology), and Hiroki Nishitani (Kansai University)

The award winners were congratulated warmly by all participants. IMFEDK will continue to encourage and contribute to our student members in the Kansai area by providing opportunities to present their ideas in English hence extend their technical network to other countries.

We will hold annual Kansai Colloquium Electron Devices Workshop in November, 2015 in Osaka to review major papers published during the last 12 months. Please visit our homepage to find out more. http://www.ieee-jp.org/section/kansai/chapter/eds/.

~Kuniyuki Kakushima, Editor

ED Malaysia Kuala Lumpur Chapter

–by Badariah Bais & Zubaida Yusoff

A workshop on publishing articles in Q1 journals was held April 7–8, 2015, from 8.00 a.m. to 5.00 p.m. at RHR Hotel UNITEN. This event was jointly organized by Functional Devices Laboratory, Institute of Advanced Technology, Universiti Putra Malaysia and the IEEE Electron Devices Society Malaysia Chapter. About 50 participants attended the workshop which was held as a platform for researchers and students to gain knowledge on how to produce high impact articles which is suitable to be published in Q1 journals. Prof. Dr. Mohd. Zobir Hussein from Universiti Putra Malaysia was invited to present tips and guidelines on this matter. At the end of the workshop about 30 articles were submitted through online submissions.

A short course on TRIZ Innovation for Industry and Research & Development was held at College of Information Technology, UNITEN from June 15-16, 2015. This course was co-organized by IEEE EDS Malaysia, COE UNITEN and IMEN, UKM. The instructors of the course were Prof. Emeritus Dr. Prakash R. Apte (College of Engineering Pune-COEP, India), and Mr. S. S. Narayan (DGM, Mahindra & Mahindra, India). The course was attended by 15 participants both from industry and academia, who were briefed on the concepts of Triz and interactive session including using Triz to solve research and industrial problems.

The IEEE ED Malaysia Chapter organized a Technical Talk by IEEE Distinguished Lecturer (DL) and IEEE Fellow, Prof. Bin Yu from the State University of New York on June 12, 2015, at Auditorium A, Kulliyyah of Engineering, International Islamic University Malaysia (IIUM). The talk on *"Graphene and Beyond: Two-Dimensional Nanomaterial Enabled Electronics,"* successfully attracted 33 participants from IIUM's staff and postgraduates and IEEE ED members. In his talk, Prof. Bin Yu has comprehensively explained how graphene (two-dimensional carbon sheet) and its derivative material systems have received significant amount of research interests from both academia and industry. The

Participants of the workshop organized by the ED Malaysia Kuala Lumpur Chapter

Participants of the short course at the College of Information Technology, UNITEN

IEEE Distinguished Lecturer and IEEE Fellow, Prof. Bin Yu (front row, center)

emerging 2D nanostructures exhibit unique electrical, optical, thermal, and electromechanical properties, attributed to their distinctive layered configuration, energy band structure, and quantum phenomena such as massless Dirac fermion transport. The talk has introduced the basic structure, material preparation methods, and potential design and implementation of logic switches / on-chip interconnects / solar cells / photodetectors on 2D material platform.

ED/CPMT/REL Singapore Chapter

–by Chee Lip Gan

It has been a busy few months at the Singapore chapter with the hosting of the EDS BoG Meeting Series from May 29th–June 1st at the Marina Mandarin Hotel. This was the second time our chapter hosted the EDS AdCom/BoG and Region 10 Chapters meetings. Our chapter provided local hospitality for the delegates. This was followed closely by the 2015 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC'2015) held in Singapore for the first time at Nanyang Technological University from June 1–4. The week was rounded off when the 47th Workshop and IEEE EDS Mini-Colloquium on NAnometer CMOS Technology (WIMNACT-47) was held June 5th with 11 Distinguished Lecturers (DLs) giving talks at the 3 local universities (National University of Singapore, Nanyang Technological University, Singapore University of Technology and Design) simultaneously. Our chapter also co-organized the Chapter's flagship conference IPFA (22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits 2015) at Hsinchu, Taiwan, June 29th–July 2nd with the IEEE EDS Taipei Chapter. Detailed conference reports are given separately.

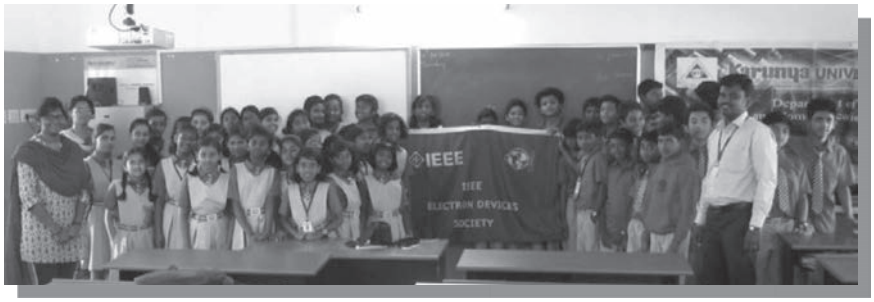
~Susthitha Menon, Editor

ED/SSCS Bangladesh Chapter

–by Saeed-Uz-Zaman Khan

The chapter jointly organized a technical talk on *"Polariton Laser: A New Frontier of Optoelectronics"* on March 23, 2015, at the Department of

Mr. Md Zunaid Baten giving his talk at BUET



Participants and instructors of school outreach program of ED Coimbatore Chapter

EEE, BUET. The talk was given by Md. Zunaid Baten, PhD Student, University of Michigan, Ann Arbor, Michigan, USA. He discussed the physics, development and application of polaritons and polariton lasers.

The chapter also organized an EDS Distinguished Lecture on *"Carbon: The Soul of Future Nanoelectronics"* on April 4, 2015,at the Department of EEE, BUET. The talk was given by Dr. Vijay K. Arora, IEEE EDS Distinguished Lecturer and Professor, University Teknologi Malaysia and Wilkes University, Pennsylvania, USA, where he discussed Nonequilibrium Arora's Distribution Function (NEADF) as the basis of transformation of randomly oriented to directed moments in the presence of an electric field, leading to saturation that is limited to the intrinsic Fermi velocity for carbon-based devices.

The chapter also jointly organized a technical talk on *"50 Years of Moore's Law: Impact and Challenges in Semiconductor Industry,"* May 27, 2015, at the Department of EEE, BUET. The talk was given by Dr. Md. Ataur Rahman Sarkar, Sr. Engineer, Intel Corporation, USA. His talk briefly covered the impact of Moore's law in semiconductor manufacturing and the challenges to overcome to keep this law alive for the years to come. Concepts of some emerging technologies such as nanowire-based devices in place of conventional CMOS technology were also presented.

ED Coimbatore Chapter

–by D. Nirmal

The ED Coimbatore chapter co-organized a 3-day Electronic Camp at Karunya Christian School, Coimbatore from April 15–17, 2015, to let more than 100 primary and secondary students, ages ranging from 10 to 15, explore the fun of electronic designs. The instructors and student helpers were all Undergraduate Electronic Engineering students in this outreach program. In the camp, the young children assembled various electronic gadgets such as running light, smart alarm, electric fuse and digital counter on breadboards using the Elenco Snap Circuits kits.

ED/CAS Hyderabad Chapter

–by Mohammed Arifuddin Sohel

The chapter organized a Distinguished Lecture program by Dr. Rajiv Joshi, Researcher, T.J. Watson Research Center, IBM, USA, on *"Technology and circuit Co design for power reduction in nano scale era."* The lecture was held at three venues i.e. Muffakham Jah College of Engineering and Technology (January 23, 2015), Vasavi Engineering College, Ibrahimbagh (January 23, 2015) and BITS Hyderabad Campus (January 24, 2015), spread over different geographical locations across the Hyderabad City for the benefit of the IEEE student members and host institutes. Dr. Joshi addressed on nanometer design challenges with special focus on planar and non-planar devices, low power design techniques employed in circuits for logic and Memory and with special focus on SRAM.

Professor Vijay K. Arora giving his talk in front of the audience at BUET

Dr. Rajiv Joshi (front row, third from left) with IEEE ED/CAS ExCom and other participants at MJCET

Workshop participants at NIST Berhampur

ED NIST Student Chapter, Berhampur
–by Ajit Kumar Panda

The chapter organized a four week workshop on ***"ASIC/ VLSI Design using CAD Tools"*** from May 12 through June, 6, 2015, at National Institute of Science & Technology, Palur Hill, Berhampur, for the fresh engineers/ researchers/ faculties to enhance the domain knowledge in VLSI Design in our region. The NIST VLSI Group with 15 experienced instructors conducted the workshop and provided their knowledge on four CAD tool like PSpice, Xilinx, Tanner and CADENCE. Nearly 200 participants from NIST, VITAM, SOA-University, and Sambalpur University from both PG and UG level attended the workshop.

AP/ED Bombay Chapter
–by V. Ramgopal Rao

The IEEE AP/ED Bombay Chapter, IIT Bombay, organized technical talks in diverse areas such as MEMS fabrication and packaging, spintronics, piezoelectronic actuation, energy harvesting, X-ray lithography and optomechanics. Some of the notable speakers were Prof. Kenji Uchino from Penn State University, USA; Dr. Roopali Kukreja from University of California, San Diego; Dr. Vibhor Singh, Delft University of Technology, Netherlands and Dr. Susthitha Menon from Institute of Microengineering and Nanoelectronics (IMEN), UKM (National University of Malaysia).

Prof. Kenji Uchino, one of the pioneers in piezoelectric actuators and the Founding Director of the International Center for Actuators and Transducers, in his talk titled *"Piezoelectric Actuator Renaissance"* reviewed the recent advances in materials, designing concepts and discussed the five key trends in this area, for providing the future perspectives; *"Performance to Reliability", "Hard to Soft", "Macro to Nano", "Homo to Hetero"* and *"Single to Multi-functional."*

Dr. Roopali Kukreja delivered a talk titled, *"X-ray imaging of spin injection into copper across a Co/Cu interface."* In her talk, she highlighted that Spin currents are believed to play a key role in the ultrafast manipulation of the magnetization by femtosecond optical pulses, like in all optical switching. Prof. Vibhor Singh's talk titled, *"Optomechanics with superconducting quantum circuits"* emphasized that Cavity optomechanics, which utilizes the interaction between light and mechanical motion has been extremely successful in detecting and controlling the mechanical motion with high sensitivities.

Prof. Kenji Uchino delivering his talk

ED Student Chapter, VIT Chennai
–by B. Lakshmi

The chapter organized a two-day workshop, March 27-28, 2015, on *"Nano Devices with Hands-on Training in TCAD"* which was attended by over 40 participants. Dr. B. Lakshmi gave two technical talks on the topics *"Device Engineering: From micro to nano- A new paradigm"* and *"Carbon Nano Tubes- Physics and Applications"* followed by hands-on training beginning with *"Introduction to TCAD"* with the

Dr. B. Lakshmi delivering his technical talk

demonstration of different modules of TCAD.

ED Calcutta Chapter

–by Swapnadip De and Soumya Pandit

The IEEE ED Kolkata Chapter, in association with the Department of Electronics and Communication Engineering, Meghnad Saha Institute of Technology, organized two DL talks by Prof. Vijay Kumar Arora on *"Overview: Trends of Nanotechnology journey"* and *"Equilibrium carrier statistics,* April 6, 2015, at Meghnad Saha Institute of Technology, Kolkata. The talks were attended by 90 participants, of which 35 were IEEE members. Two more DL Talks on *"Non equilibrium carrier statistics"* and *"Carbon-The soul of future Nano electronics"* by Prof. Vijay Kumar Arora were also organized by the Chapter, in association with the Department of ECE, Meghnad Saha Institute of Technology, April 7, 2015, at Meghnad Saha Institute of Technology, Kolkata. The talks were attended by 75 participants, of which 10 were IEEE members.

The IEEE Kolkata Section, IEEE Electron Devices Society Kolkata Chapter, IEEE EDS HITK Student Branch Chapter, IEEE EDS KGEC Student Branch Chapter and IEEE EDS CU Student Branch Chapter in association with the Department of ECE, Heritage Institute of Technology, organized a Distinguished Lecture program at AV Hall of Heritage Institute of Technology on April 17, 2015, on *"Importance of Calibration in Quality Assurance"* by Prof. Sivaji Chakravorti, Distinguished Lecturer, IEEE Power & Energy Society and Professor of the Department of Electrical Engineering, Jadavpur University. The second DL on "Design Challenges for Low Power VLSI Circuits" was presented by Professor Subir Kumar Sarkar, IEEE EDS Distinguished Lecturer and Professor, Department of ETCE, Jadavpur University. These distinguished lectures were attended by more than 105 students and 15 faculty members.

ED Student Chapter, IIT Roorkee

–by Om Prakash

The chapter organized a workshop on *"MEMs Prototyping, RF MEMs Fabrication, Design and Modeling,"* May 9, 2015, at the Electronics & Communication Engineering Department of IIT Roorkee, which was attended by around 55 participants including Faculty, Research Scholars and graduate students.

Dr. Sudhir Chandra Professor, Center for Applied Research in Electronics, IIT Delhi, focused on *"MEMS Research, development Prototyping: Challenges for Academic Institution"* and then Dr. Kamal J. Ranga, Chief Scientist and Professor ACSIR, Sensors & Nano –Technology Group,CEERI, Pilani, spoke on *"Surface Micro – Machined RF MEMS and Test Structures."* After lunch, Dr. M. M Joglekar Assistant Professor, Department of Mechanical

Prof. Vijay Kr. Arora at the Inaugural ceremony of the IEEE EDS DL program at MSIT, April 6–7, 2015

Speakers and attendees at the IEEE ED workshop held on May 9, 2015, at IIT Roorkee

Prof. Sivaji Chakravorti delivering his DL at Heritage Institute of Technology

IEEE ED workshop held on June 10, 2015 at IIT Roorkee

Engineering, IIT Roorkee, gave a talk entitled, *"Open loop control of electrostatically driven MEMS using a command-shaping approach."* The final distinguished lecture was given by Dr. N. P. Pathak, Associate Professor Department of Elec. & Comm. Engg., IIT Roorkee.

The chapter also organized a workshop on *"GaN Devices Fabrication, Device Modeling and Power Amplifier Design,"* May 10, 2015. The invited talks focusing on GaN devices fabrication, modeling and power amplifier design. The upcoming approach of RF power amplifier (PA) design requires embedding device model, where, access to the device intrinsic current source can provide designers new paradigm in PA design.

Prof. Patrick Roblin Dept. Electrical & Computer Engineering, Ohio State University and Dr. Seema Vinayak, Solid State Physics Laboratory, Defense Research & Development Organization, presented the talk. A live demonstration and hands-on over device measurement and characterization was presented by Keysight Technology.

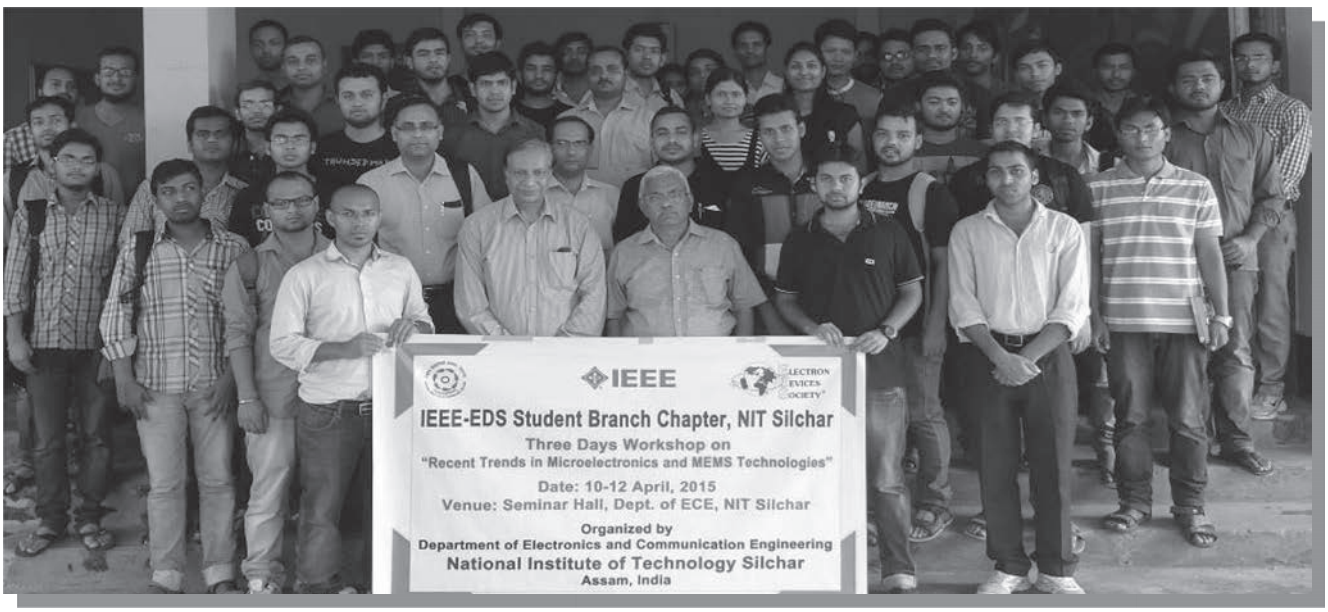
ED Student Chapter NIT Silchar

–by T. R. Lenka

The IEEE ED Student Branch Chapter – National Institute of Technology Silchar, Assam, India, organized a one-day workshop on "MEMS," February 7, 2015, in the Department of Electronics and Communication Engineering, NIT Silchar. Mr. Gaurav Saxena, IIT Guwahati and Mr. Nagesh Ch., IIT Guwahati delivered expert talks on MEMS. B.Tech/M.Tech and PhD scholars of the Department of ECE, NIT Silchar attended the workshop.

The IEEE ED Student Branch Chapter at National Institute of Technology, Silchar, organized a three day Workshop on *"Recent Trends in Microelectronics & MEMS Technologies"* from [h] April 10–12, 2015 at Department of Electronics and Communication

(from left) Mr. Nagesh Ch, Dr. A K Sunaniya, Mr. G. P. Keshri, Dr. Taimoor Khan, Dr. R. H. Laskar, Prof. F. A. Talukdar (Branch Counselor), Dr. T. R. Lenka (Chair), Mr. Koushik Guha (Coordinator), Mr. Gaurav Saxena and attendees of the Workshop held February 7, 2015



(from left) Dr. T. R. Lenka (Chair), Prof. Sudhir Chandra, Dr. Taimoor Khan, Dr. R. H. Laskar, Prof. N. V. Deshpande (Director, NIT Silchar) and attendees of the Workshop on "MEMS"

Engineering, National Institute Technology Silchar. Prof. Sudhir Chandra, Indian Institute of Technology Delhi delivered a series of talks on Microelectronics Technology, Microelectronics Fabrication & MEMS Technology. B.Tech, M.Tech and PhD scholars of the Department of Electronics and Communication Engineering, NIT Silchar, attended the workshop.

ED Delhi Chapter
–by Manoj Saxena

The chapter organized a one-day interactive session on Silvaco Full flow design tools for all semiconductor technologies on April 13, 2015, at University of Delhi South Campus, New Delhi.

Mr. Iliya Pesic, Chairman, Silvaco Inc., and Mark Maurer, Vice President Business Development, Foundry & PDK, Silvaco, along with Dr. P. K. Saxena, India Regional Head, Silvaco Singapore Pte. Ltd., delivered technical talks which were attended by over 30 participants from the Delhi and NCR region.

~Manoj Saxena, Editor

Speakers and attendees after the Interactive session held on April 13, 2015 at UDSC, New Delhi

IMPORTANT REMINDER TO CHAPTER MEMBERS

- CHANGES TO CHAPTER OFFICERS NEED TO BE SUBMITTED TO BOTH IEEE AND EDS
- PLEASE REPORT CHANGES TO IEEE VIA THE VTOOLS.OFFICERREPORTING TOOL (ACCESS TO THE TOOL REQUIRES USE OF AN IEEE ACCOUNT)
- TO REPORT OFFICER CHANGES TO EDS, PLEASE SUBMIT A CHAPTER CHAIR UPDATE FORM: https://ieeeforms.wufoo.com/forms/pgu6n1i1ixepnu/

EDS MEETINGS CALENDAR

The complete EDS Calendar can be found at our web site: http://eds.ieee.org. Please visit.

2015 37th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)	27 Sep - 02 Oct 2015	Peppermill Resort Hotel 2707 South Virginia Street Reno, NV, USA
2015 International Conference on Planarization/CMP Technology (ICPT)	30 Sep - 02 Oct 2015	Wild Horse Pass & Casino Hotel 5040 Wild Horse Pass Blvd, Chandler, AZ, USA
2015 Fourth Berkeley Symposium on Energy Efficient Electronic Systems (E3S)	01 Oct - 02 Oct 2015	University of California, Berkeley Sutardja Dai Hall Banatao Auditorium Berkeley, CA, USA
2015 26th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF)	05 Oct - 09 Oct 2015	Centre de Congrès Pierre Baudis 11, esplanade Compans Cafarelli TOULOUSE, France
2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	05 Oct - 08 Oct 2015	DoubleTree by Hilton Sonoma Wine Country One DoubleTree Drive Rohnert Park, CA, USA
2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)	11 Oct - 14 Oct 2015	Sheraton New Orleans Hotel 500 Canal Street New Orleans, LA, USA
2015 IEEE International Integrated Reliability Workshop (IIRW)	11 Oct - 15 Oct 2015	Stanford Sierra Conference Center 130 Fallen Leaf Road South Lake Tahoe, CA, USA

2015 15th Non-Volatile Memory Technology Symposium (NVMTS)	12 Oct - 14 Oct 2015	Tsinghua University Haidian District Beijing, China
2015 International Semiconductor Conference (CAS)	12 Oct - 14 Oct 2015	Hotel Rina Sinaia Bd. Carol I, Nr 8, Sinaia, Romania
2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM	26 Oct - 28 Oct 2015	Hyatt Boston Harbor 101 Harborside Drive Boston, MA, USA
2015 12th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE)	28 Oct - 30 Oct 2015	Centro de investigación y de Estudios Avanzados del IPN (Cinvestav) Av. Instituto Politécnico Nacional 2508 Col San Pedro Zacatenco Del. Gustavo A. Madero Mexico City, Mexico
2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)	02 Nov - 04 Nov 2015	The Inn at Virginia Tech 901 Prices Fork Road Blacksburg, VA, USA
2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	02 Nov - 06 Nov 2015	Doubletree Hotel Austin, TX, USA
2015 IEEE 46th Semiconductor Interface Specialists Conference (SISC)	02 Dec - 05 Dec 2015	The Key Bridge Marriott 1401 Lee Highway Arlington, VA, USA
2015 IEEE International Electron Devices Meeting (IEDM)	07 Dec - 09 Dec 2015	Hilton Washington Washington, DC, USA

2016 International Conference on Microelectronic Test Structures (ICMTS) Abstract submission deadline: 16 Oct 2015 Final submission deadline: 29 Jan 2016	28 Mar - 31 Mar 2016	Mielparque Yokohama 16 Yamashita-cho Naka-ku, Yokohama-shi Kanagawa, Japan
2016 IEEE International Reliability Physics Symposium (IRPS) Abstract submission deadline: 12 Oct 2015 Full Paper Submission deadline: 06 Mar 2015 Notification of acceptance date: 15 Dec 2014	17 Apr - 21 Apr 2016	Pasadena Convention Center Pasadena, CA, USA
2016 IEEE International Vacuum Electronics Conference (IVEC)	19 Apr - 21 Apr 2016	Monterey Marriott 350 Calle Principal Monterey, CA, USA
2016 IEEE International Memory Workshop (IMW) Abstract submission deadline: 08 Feb 2016 Full Paper Submission deadline: 08 Feb 2016 Final submission deadline: 15 Mar 2016 Notification of acceptance date: 01 Mar 2016	08 May - 11 May 2016	Paris, France
2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC) Abstract submission deadline: 22 Jan 2016	05 Jun - 10 Jun 2016	Oregon Convention Center 77 NE Martin Luther King Jr. Blvd. Portland, OR, USA
2016 28th International Symposium on Power Semiconductor Devices and IC's (ISPSD)	12 Jun - 16 Jun 2016	Zofin Palace Slovanský ostrov 226 Prague, Czech Republic
2016 IEEE Symposium on VLSI Technology	14 Jun - 16 Jun 2016	Hilton Hawaiian Village 2005 Kalia Road Honolulu, HI, USA

2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) Abstract submission deadline: 01 May 2016 Final submission deadline: 15 Jul 2016 Notification of acceptance date: 30 May 2016	23 Oct - 26 Oct 2016	Doubletree by Hilton Austin 6505 N IH 35 Austin, TX, USA
2016 IEEE International Electron Devices Meeting (IEDM)	01 Dec - 09 Dec 2016	Hilton San Francisco San Francisco, CA, USA
2016 IEEE 47th Semiconductor Interface Specialists Conference (SISC) Abstract submission deadline: 14 Aug 2016 Notification of acceptance date: 18 Sep 2016	07 Dec - 10 Dec 2016	Catamaran Resort Hotel 3999 Mission Blvd. San Diego, CA, USA
2017 IEEE International Reliability Physics Symposium (IRPS) Abstract submission deadline: 30 Sep 2016 Final submission deadline: 01 Feb 2017 Notification of acceptance date: 21 Dec 2016	02 Apr - 06 Apr 2017	Hyatt Regency Monterey One Old Golf Course Road Monterey, CA, USA
2017 IEEE 44th Photovoltaic Specialists Conference (PVSC)	25 Jun - 30 Jun 2017	Marriott Washington Wardman Park 2660 Woodley Road NW Washington, DC, USA
2017 IEEE International Electron Devices Meeting (IEDM) Abstract submission deadline: 01 Jun 2017 Final submission deadline: 01 Sep 2017 Notification of acceptance date: 01 Aug 2017	04 Dec - 06 Dec 2017	Hilton San Francisco Union Square San Francisco, CA, USA
2016 28th International Symposium on Power Semiconductor Devices and IC's (ISPSD)	12 Jun - 16 Jun 2016	Zofin Palace Slovanský ostrov 226 Prague, Czech Republic

Dear EDS Member:

The IEEE Electron Devices Society is a vibrant, prolific organization whose members make vital contributions to the global technical community each year. To ensure our members' work is properly recognized, we encourage you to nominate fellow members for our annual awards. It is in this vein that we would like to draw your attention to the awards listed to the right.

These highly prestigious awards draw nominations from all over the world. Please visit the EDS awards page on the Society website. You can find important information about eligibility, deadlines and other details.* If you need more information or have a question about preparing a nomination, please contact Laura Riello of the EDS Executive Office, l.riello@ieee.org. We strive to maintain a comprehensive set of awards which is representative of our member activities. As the field of electron device engineering evolves, so too must our awards. If you would like to suggest new awards, we would welcome your comments and suggestions.

Sincerely,

Paul Yu
EDS Awards Committee Chair

EDS President, Albert Wang, presents Joachim Burghartz with the 2014 EDS J.J. Ebers Award

- Robert Bosch Award
- J.J. Ebers Award
- Distinguished Service Award
- Education Award
- Early Career Award
- PhD Student Fellowship
- Masters Student Fellowship
- Chapter of the Year Award

Visit the EDS Website

*Please Note: Although the IEEE Electron Devices Society (EDS) is pleased to invite all individuals and groups in the OFAC embargoed countries to submit nominations for IEEE EDS Awards, the IEEE EDS cannot provide any award monies to members from such countries at this time.

EDS Vision and Mission Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.