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Technical Briefs

Emergence of Memtronics: From Memory to Sensor, Logic and Display

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Memory materials have recently been used not only in data storage, but also in emerging applications in data sensing, processing and display. What properties do these bistable materials have that attract their pervasive use in all the major functional areas of future electronic devices?

Information sensing, processing, storing, and displaying are the four fundamental functions of electronic devices. Whether it is a transistor for logic operations, a flash memory for data storage, a light emitting diode for display devices, or an ion-sensitive switch for biosensing applications, until now these key functional devices have been made of different combinations of metallic/semiconducting/insulating materials. Recently, however, many of the emerging devices/architectures [1] are beginning to use *bistable (non-volatile) memory materials* or analogous bistable structures (e.g., NEMS) to achieve superior performance. These include neuromorphic [2] and logic-in-memory architectures [3], nanomagnetic and spintronic devices [4, 5], negative capacitance transistors [6], NEMS switch [7], atomic switch [8], correlated electron devices [9], electrophoretic and other bistable passive displays [10–12], bifurcation based chemical and biosensors [13, 14], etc. A close examination reveals that such *widespread use of memory structures in data sensing, processing, storing and displaying* (as we refer by the term "memtronics", signifying memory electronics) is not a mere coincidence. In the following, we will list a few intrinsic properties of these materials that encourage their ubiquitous use in such a broader range of applications.

(1) A binary logic device works by defining two states that are isolated by an "energy barrier" created by some physical means within the system [15, 16]. The input information conditionally

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Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at radhakrishnan@ieee.org

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Emergence of Memtronics

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lowers the barrier so that the relative occupancy of the states can be altered. For traditional semiconductor devices, the barrier is created *macroscopically* by stacking different semiconductor materials, oxides, metals, etc. For example, gate metal, oxide layers, and semiconductor channel form the required barriers in a flash memory (Fig. 1(a)). Similarly, the channel forms the energy barrier from source to drain in a MOSFET [15]. The physical design of energy landscape using different materials in this heterogeneous manner leads to a certain minimum scaling limit. This is because the integrity of both the materials and/or the devices are degraded at very small length scales due to, for example, random dopant fluctuations, short channel effects, etc. In contrast, the required energy barrier is intrinsically built-in within any memory material (Fig. 1(a)). Thus, a single homogeneous material, can act as a switch or memory, and ideally, the element can scale down to a much smaller limit [17], overcoming the density scaling challenge associated with classical semiconductor devices. Some of the *beyond CMOS* devices, such as nanomagnetic logic [4] (e.g., Magnetic Quantum Cellular Automata (MQCA) [18]) exploit this **intrinsic energy barrier** of the memory materials to promise high density logic/memory devices for future electronics.

(2) Another problem of the existing semiconductor devices relates to the excessive energy neces-

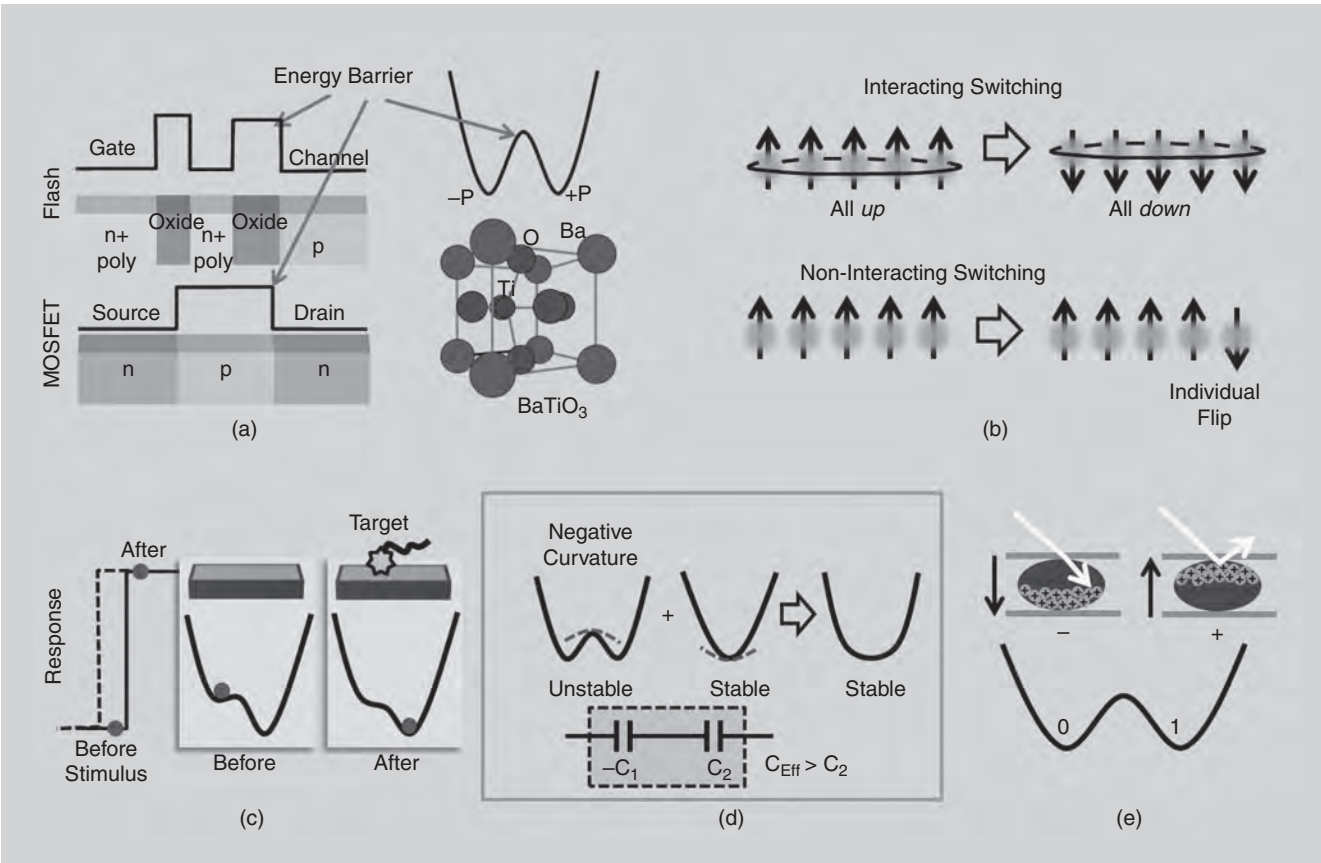

Fig. 1. (a) Energy barrier in traditional semiconductor devices (shown for flash memory and MOSFET) are created macroscopically by connecting different semiconductor/insulator materials. This barrier can be intrinsically present in a memory material as illustrated using a ferroelectric crystal ($BaTiO_3$) where the Ti atoms stay in one of the two energy pockets below the Curie temperature. (b) With interacting switching in a magnetic nanodot, a large number of spins are "stitched" together and switch like a single entity. If those were non-interacting, individual spins could be flipped, making those more vulnerable to thermal noise. (c) Due to the extreme nonlinearity of a bifurcation based sensing device, the capture of a tiny bit of target molecule can cause a sudden jump in the response signal. (d) When biased properly with a stable system (positive capacitance), the unstable equilibrium state of a memory material (negative capacitance) can give unconventional performance boost to traditional devices, such as increasing the gate capacitance of a transistor, etc. (e) Memory structures can have optically distinguishable states as used in an electrophoretic display.

sary to switch between the states. This challenge originates from the greater degree of freedom of the electronic charges which translates to lesser immunity to thermal noises. For example, the minimum switching energy for N electronic charges is given by DE_B, where $E_B = k_B T ln(r)$ is the minimum energy barrier height necessary to define binary states with an error probability of $1/r$ [15], and (D~N) is the degree of freedom for the charges. Thus, the minimum voltage margin is E_B/q (~0.4 V for $r = (I_{ON}/I_{OFF}) = 10^7$). However, for some of the memory materials, the switching of the state variables occurs collectively, which reduces the degree of freedom. For example, during a switching event, all the spins (large N) in a nanomagnet work in unison ($D \sim 1$) [19] (Fig. 1(b)). In such case, the minimum energy dissipation per switching is of the order of E_B (instead of NE_B). Many of the nanomagnetic and spintronic devices promise energy scaling by several orders of magnitude [4] by utilizing this **interacting switching** of memory materials.

Interestingly, the interacting switching property is also present in other bistable memory structures, such as a NEMS. In this case, the charges are constrained mechanically within a given mass (electrode) and the degree of freedom reduces to the order of one. As a result, N charges can be switched from one state to the next with a very small difference in the applied voltage (E_B/Nq, instead of E_B/q for a non-interacting system), which is characterized essentially by a *sudden jump* during the switching of a NEMS. In addition to low power logic and memory applications [1], this extreme **non-linear transition** is the basis of bifurcation based chemical and biosensing techniques which promise attogram-scale mass sensing in atmospheric conditions [13, 14]. Here the system can be biased very close to the bifurcation point in a metastable way and the arrival/detection of the target causes a sudden jump across the critical point (Fig. 1(c)).

(3) Another feature of memory structures, which is not very obvious at first, is the presence of **unstable equilibrium states** in between a pair of stable states (Fig. 1(d)). Although these unstable states are generally inaccessible (and hence not very useful), one can bias a memory material at the unstable state by combining it with another stable material. In the combined system, the former acts as a negative circuit element (e.g., negative capacitor for case of ferroelectrics) which can potentially enhance the performance of the traditional devices and circuits in a very unique way. The proposed negative capacitance field effect transistor [6] and the ferroelectric-NEMS [20] utilize this property to amplify the applied voltage for a sub-60 mV/decade switching and sub-1 V pull-in voltage, respectively.

(4) The most recognized property of nonvolatile memory is the **bistability** which not only enables various data storage applications, but also reduces power consumption during off state in a logic switch. In addition, if a memory element has optically distinguishable discrete states (Fig. 1(e)), it can be used as a superior quality passive display element. This includes electrophoretic, droplet-driven electrowetting, bistable electrofluidic, bistable LCD, MEMS-based display, etc. [10, 11], which work using the ambient light (like ink on a paper) and the only energy required is during the switching of the display pixel. This can potentially save significant amount of power in many portable electronic devices.

(5) Finally, the intrinsic scalability of memory materials enables the design of logic devices with memory as an elemental and integrated building block. In other words, one can squeeze a memory functionality into the design of a logic device which was not practical with previous generations of heterogeneous non-volatile memories due to their relatively larger size. These revamped beyond-Neumann logic designs, such as adaptive, neuromorthic logic [2] and logic-in-memory [3] architectures, which promise a paradigm shift in computation, and reduced transmission loss.

These are some reasons that inspired widespread use of bistable memory structures in different electronic devices (sensor, logic, memory, display). Since all of these devices possess analogous double well energy landscapes, one must take advantage of this connection across the disciplines, and share inventions and solution strategies of one field to the other. In fact, such efforts have already led to the realization that the negative capacitance scheme [6], originally developed for logic, can also be used in NEMS or bistable display applications [20]. In addition to such cross-disciplinary research, one must also focus on defining the primary challenges towards developing these memtronic devices/architectures. For example, one may identify the reduced speed and the inefficient switching [21] of some memory materials due to domain formation, interfacial defects, grain boundaries, etc. Note that the unprecedented development of semiconductor technology has been possible partly due to the ability to grow the single crystalline materials and improve the quality of the interfaces. Likewise, one needs to develop low defect density memory materials and integrate these in the future low power memtronic devices. The technological barriers, without any doubt, are challenging, but once the functionality and performance are promised, it is highly likely that these barriers would be overcome.

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EDS Tutorials at Semicon West 2016

By Mukta Farooq

EDS coordinated a half-day session at Semicon West 2016, held in the Moscone Center in San Francisco on July 14th, as part of the overall Semicon West 2016 Business and Technology Conference. This was a paid session, with IEEE EDS members receiving a discount code for registration. Both tutorials were well attended with over 70 people in each session.

Tutorial: 2.5D/3D Integration Technology

Instructor: Mukta Farooq, Ph.D., GlobalFoundries Fellow and IEEE Fellow.

2.5D/3D integration technology encompasses a wide variety of configurations which employ TSVs (Through Silicon/Substrate Vias) in a silicon wafer. 2.5D generally refers to heterogeneous integration of chips using interposers which typically have only passive components: wiring, capacitors and inductors. 3D technology goes beyond the interposer by integrating logic functionality in the assembly. 3D integration has the ability to enhance system performance by increasing bandwidth, reducing wire delay, and enabling better power management. In 3D technology, the TSVs may be integrated into the CMOS transistor fabrication at a number of points in the manufacturing sequence. Key considerations to determine the optimal introduction point include the size of the TSV, dimensional compatibility of the TSV with the BEOL (Back End Of Line) features, and the wiring design requirements. In this tutorial, we will review the various types of 2.5D and 3D integration, and why they offer significant advantages over conventional methods. We will also discuss the key elements of TSV fabrication including via etching, insulation, metallization, annealing, capping, as well as wafer grindside processing. We will also discuss the effects of TSVs on devices and BEOL structures, and the type of reliability testing that is required to evaluate the long-term impact of TSVs.

Tutorial: GaN Devices and Technology

Instructor: Patrick Fay, Ph.D., Professor, Dept. of Electrical Engineering, University of Notre Dame.

The unique material properties of GaN and related materials provide significant opportunities for realizing exceptional levels of device performance, both for conventional devices such as HEMTs and HFETs, as well as for novel and potentially disruptive device designs. These devices show promise for both existing as well as emerging applications. Current applications for GaN devices include power conversion and control as well as RF power amplification, while potential future applications include high-performance mixed-signal, millimeter-wave, and sensing applications, to name just a few. GaN-based device concepts to address the specific needs of each of these areas are under intensive development by groups around the world. This course will provide a broad overview of the material properties, device structures, fabrication processing issues, and applications surrounding this emerging device technology. At the material properties level, the III-N compounds offer several unique features that are important to achieving optimum device performance. The physical origins of these fundamental material properties – and how these properties differ in important ways from other semiconductor material systems – will be described. Device structures that leverage these unique properties of GaN and related materials, including HEMTs and HFETs, homojunction and heterojunction diodes, and a range of vertical FET concepts, will be described and their strengths and limitations for applications will be explored. This discussion will also include an overview of fabrication process technology, scaling trends, the impact of process modules on device performance and characteristics, and key technological issues. Applications for these device technologies will be discussed, and the prospects for future application spaces for nitride-based devices will be examined.

Upcoming Technical Meetings

2016 IEEE International Electron Devices Meeting: Program Highlights

The 62nd annual IEEE International Electron Devices Meeting (IEDM), to be held December 3–7, 2016, in San Francisco, California, USA, will have various Special Focus Sessions, Tutorials and Workshops. Details of these events include:

Special Focus Sessions

- **Wearable Electronics and Internet of Things (IoT)** – Wearable technology offers great promise for communications, fitness tracking, health monitoring, speech therapy, elder care/assisted living and many other applications. This Special Focus Session has been organized to benchmark wearable electronics technologies, to address applications with comprehensive system demonstrations, and to learn industrial perspectives about the gaps, challenges and opportunities for wider uses of wearable and IoT technologies. Papers on flexible/stretchable electronics, MEMs, display devices, sensors, printed electronics, organic devices and 2-D material devices enabling wearables/IoT devices also will be featured.
- **Quantum Computing** – As traditional CMOS scaling enters the post-Moore's Law era, quantum computing has emerged as a possible candidate for further device scaling because it exploits the laws of quantum physics and may make much more powerful computers possible. This Special Focus Session will explore relevant semiconductor-related fabrication issues and will brainstorm R&D directions for new materials, devices, circuits, and manufacturing approaches for the scalable integration of a large number of qubits with CMOS technology, operating at cryogenic temperatures for the realization of quantum computers.
- **System-Level Impact of Power Devices** – While there are forums that serve circuit experts for the exchange of ideas and the reporting of breakthroughs, there hasn't been a suitable forum for bringing device and circuit experts together to consider impacts at the system level, even though that would be fruitful due to the interactions of circuits and devices. IEDM aims to serve as the forum for their dialogue, and so this Special Focus Session has been organized. Papers are expected to explore the system-level impact of power devices, and also to describe various types of power devices targeting the full range of power/power conversion applications such as hybrid vehicles, utility and grid control, computing/telecom power supplies, motor drives, and wireless power transfer.
- **Ultra-High-Speed Electronics** – There have been many advances and breakthroughs in ultra-high-speed electronics for communications, security and imaging applications, but technology gaps continue to prevent spectrum above millimeter-wave frequencies from being fully used. This Special Focus Session has been organized to discuss, showcase and benchmark advanced ultra-high speed devices and circuits based on high-electron-mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs) and conventional CMOS devices; high-speed interconnect; antennas for ultra-

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high-speed systems; ultra-high-frequency oscillators; and to discuss other possible applications.

Tutorials

A program of 90-minute tutorial sessions on emerging technologies will be presented by experts in the fields, to bridge the gap between textbook-level knowledge and leading-edge current research. Advance registration is recommended.

- **The Struggle to Keep Scaling BEOL, and What We Can Do Next**, *Dr. Rod Augur, GlobalFoundries* – Looking ahead, it's the interconnect that threatens further cost-effective scaling. The tutorial will cover challenges and trade-offs in back-end-of-the-line (BEOL) scaling, and will evaluate emerging devices from a scaled-BEOL viewpoint.
- **Electronic Circuits and Architectures for Neuromorphic Computing Platforms**, *Prof. Giacomo Indiveri, University of Zurich and ETH Zurich* – The principles and origins of neuromorphic (i.e., brain-inspired) engineering, examples of neuromorphic circuits, how neural network architectures can be used to build large-scale multi-core neuromorphic processors, and some specific application areas well-suited for neuromorphic computing technologies will be discussed.
- **Physical Characterization of Advanced Devices**, *Prof. Robert Wallace, Univ. Texas at Dallas* – Physics, and chemistry that enable modern physical characterization of novel electronic materials will be covered. How these techniques can shed light on electronic materials research and development, and on the resultant devices. Examples of novel electronic materials for device applications and techniques discussed will include high-resolution electron microscopy, scanning tunneling microscopy and spectroscopy, dynamic x-ray photoelectron spectroscopy, and ion mass spectrometry. The detection limits of these techniques and its relation to device behavior.
- **Present and Future of FEOL Reliability – from Dielectric Trap Properties to Reliable Circuit Operation**, *Dr. Ben Kaczer, IMEC* – This tutorial will introduce the main degradation mechanisms occurring in present-day CMOS. The reliability of novel devices (SiGe, IIIV, gate-all-around nanowires, junctionless FETs, tunnel FETs), of deeply-scaled devices, and of circuits (e.g., "reliability-aware" designs) will be covered in detail. The tutorial will give attendees an overview and background in this area sufficient to allow them to follow and participate in any discussion on reliability in general and on front-end-of-the-line (FEOL) reliability in particular.
- **Spinelectronics: From Basic Phenomena to Magnetoresistive Memory (MRAM) Applications**, *Dr. Bernard Dieny, Spintec CEA* – Spintronics phenomena, magnetic tunnel junctions (growth, magnetic and transport properties), field-written MRAM (toggle and thermally assisted MRAM), STT-MRAM (principle and development), 3-terminal MRAM and innovative architectures that benefit from these high-endurance non-volatile memories will be covered.
- **Technologies for IoT and Wearable Applications, Including Advances in Cost-Effective and Reliable Embedded Non-Volatile Memories**, *Dr. Ali Keshavarzi, Cypress Semiconductor* – A range of technology opportunities for IoT and wearable applications, including embedded non-volatile memories (eNVM), IPs and integrated solutions based on charge-trap memory technologies such as SONOS for low power (LP) and ultra-low-power (ULP) for advanced technology nodes are included. Technologies will be described for various integrated IoT, wearable and energy-harvesting systems using programmable systems-on-chips (SoCs) with digital and analog capabilities, along with low-energy Bluetooth radio, WiFi radio, solar cells, sensors, actuators, and power management ICs will be described.

Short Courses

The Short Courses provide the opportunity to learn about important areas and developments, and to benefit from direct contact with world experts. Advance registration is recommended.

1. **Technology Options at the 5-Nanometer Node**: This course will describe the complex technological challenges at the 5nm node and explore innovative potential solutions. It begins with an in-depth discussion of patterning strategies being pursued to print critical features. Then, a pair of lectures will provide an overview of current transistor technologies and their relative strengths/weaknesses in the context of various applications such as mobility, data centers and IoT. Strategies for effective mitigation of performance-limiting parasitic resistance and capacitance will be discussed, and advanced interconnect technologies including post-copper materials options for BEOL and MEOL applications will be addressed. Lastly, metrology challenges for in-line and end-of-line process technologies will be discussed. The intent of the course is to provide a thorough understanding in process technology targets at the 5nm node and their potential solutions. Attendees will have the opportunity to learn about advanced technology options that are being actively pursued in the industry from leading technologists.

   This course consists of lectures from six distinguished speakers:

- Nano Patterning Challenges at the 5 nm Node, *Akihisa Sekiguchi, Tokyo Electron, Japan*
- Novel Channel Materials for High-Performance and Low-Power CMOS, *Nadine Collaert, IMEC*
- Transistor Options & Challenges

for 5 nm Technology, *Aaron Thean, National University of Singapore*

- Low Resistance Contacts to Enable 5 nm Node Technology: Patterning, Etch, Clean, Metallization and Device Performance, *Reza Arghavani, Lam Research, USA*
- Parasitic R and C Mitigation Options for BEOL and MOL in N5 Technology, *Theodorus Standaert, IBM, USA*
- Metrology Challenges for 5nm Technology, *Ofer Adan, Applied Materials, Israel*

2. **Design/Technology Enablers for Computing Applications** – This course will describe how various design techniques and process technologies can enable computing applications, beginning with the relative advantages and disadvantages of processors such as CPU, GPU and FPGA with regard to today's high data demands. It then will cover how memory becomes a bottleneck, and will discuss various emerging memory technologies to mitigate the problem. Because managing power dissipation has become critical, it also will offer a broad perspective on power efficiency in computing and how interconnect plays a pivotal role in both performance and energy efficiency. Finally, 2.5-D and 3-D advanced packaging technology is discussed for system integration.

This course consists of lectures from five distinguished speakers:

- The Rise of Massively Parallel Processing: Why the Demands of Big Data and Power Efficiency are Changing the Computing Landscape, *Liam Madden, Xilinx, USA*
- Breaking the Memory Bottleneck in Computing Applications with Emerging Memory Technologies: a Design and Technology Perspective, *Gabriel Molas, Leti, France*
- Power Management with Integrated Power Devices and how GaN Changes the Story, *Alberto Doronzo, Texas Instruments, USA*
- Interconnect Challenges for Future Computing, *William J. Dally, NVIDIA & Stanford, USA*
- Advanced Packaging Technologies for System Integration, *Douglas Yu, TSMC, Taiwan*

For Further information about IEDM, Registration, etc., visit www.ieee-iedm.org.

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1st Electron Devices Technology and Manufacturing Conference (EDTM)

Toyama International Conference Center, Toyama, Japan
February 28th to March 2nd, 2017

IEEE Electron Devices Technology and Manufacturing Conference (EDTM): The Inaugural EDTM (Electron Devices Technology and Manufacturing) conference is a full three-day conference to be held at Toyama International Conference Center, Japan from February 28th to March 2nd, 2017, fully sponsored by the IEEE Electron Devices Society (EDS). As semiconductor technology scaling challenges continues to grow, so should the industries collaborative efforts to overcome them must increase. EDTM is intended to serve as a forum for the electron devices community to collaborate on topics ranging from devices, materials, and tools, to create new and innovative technologies. EDTM will provide the following new formats.

1. Technical sessions

EDTM 2017 and beyond will have a strong specific technical focus, and this year's focus being on devices and process technologies for advanced applications, IoE (Internet of Everything) and related low-power devices, advanced memories, sensors, actuators, MEMS, bio.-chips, passive devices, and all types of (exploratory) devices related to advance applications and IoE. Papers/Posters on materials and processes for enabling above-mentioned devices building in heterogeneous integration such as 2.1, 2.5 and 3D structures using wafer-level packaging process (*e.g.*) are of great focus.

EDTM aims for highest quality, and all papers accepted would be subject to IEEE-EDS standard review processes and conference publishing guidelines. Accepted and presented papers will be published in EDTM proceedings. A selected number of high impact EDTM papers would be invited for the consideration of publication in the *IEEE Journal of Electron Devices Society* (J-EDS) as extended version of EDTM conference papers following the IEEE publication policy and J-EDS author-guidelines.

2. Education

- *Tutorials*: We will provide both the basic and advanced programs. Basic program will be presented in local language.
- *Poster sessions*: Primarily intended for young engineers and

students. The best poster will be awarded in the conference.

- *Short courses*: Will bring high level programs.

3. Exhibition

Given the strong semiconductor manufacturing base in Asia, we intend to offer exhibits that will demonstrate products and technology. All of the exhibitors will have an opportunity to offer technical insight and share their knowhow. Moreover, we hope to offer Forum Making Session to engage and allow deeper discussions between device, material, and equipment engineers and technologists.

Following areas will be covered in the conference for which papers are solicited till November 4, 2016:

Devices and Manufacturing for "Cloud and Edge:" papers in all areas of device and manufacturing enhancing cloud and edge computing; high-performance devices include CMOS technology, platform technologies, stand-alone and embedded memory technologies, interconnects, optical interconnects, compound semiconductors, low-dimensional systems including 2D materials, nanowires, nanotubes, and quantum dots, 3D-IC. The devices for edge computing correspond to ultra-low power devices, energy harvester, RF devices, sensors, sensor networks, display, and actuators, MEMS, power devices, flexible and stretchable electronics, printed electronics, organic and inorganic displays.

Papers are also solicited on the manufacturing issues on process control, manufacturability, yield improvements, and failure analysis and related considerations.

Packaging and Manufacturing for "Cloud and Edge:" papers in all areas of advanced packaging and package-related manufacturing technologies for both cloud and edge applications of IoT, especially, heterogeneous integration technologies such as 2.1D, 2.5D and 3D integrations, wafer-level packaging and panel-level packaging are strongly encouraged; breakthrough technologies in ultra-fine-pitch interconnection, sub-micron package-level wiring, optical/wireless interconnect, power/sensor device packaging, control in thermal-expansion coefficient and thermal management are also recommended; package design methodology and technique for miniaturization of IoT edge sub-systems, and the manufacturability of all the technologies above are of course interested. Emerging topics, such as bio-compatible package, neuromorphic interconnection, and flexible/bendable package are very much welcome.

Process, Tools, and Manufacturing: papers in all areas of process, tools, and manufacturing systems with novel sensing technologies and artificial-intelligence and deep-learning algorithms; process and equipment including process module, process integration and process control, and equipment that improve device performance, reliability, yield or enabling new product are also solicited; the topics are substrates, isolation technologies, integration of heterogeneous channel materials, dielectrics and metal electrodes for gate stacks and MIM capacitors, shallow junctions, and silicides, low dielectric constant materials, contact and via processes, multi-patterning and EUV lithography, self-assembly techniques, deposition techniques include CVD, ALD and PVD, dry and wet etch techniques, cleaning, planarization, integration process for sensors, MEMS, RF devices, and photonics electronics, and process and tool design or process control techniques to reduce variation or improve reliability or yield.

Materials: papers in all areas of materials to achieve the higher performance and manufacturability, including materials for the deposition of films of semiconductor, magnetics, ferroelectrics, insulators, metals, liquid crystals are highly welcome; and to achieve their structures, the resist, organic films, etching gas, and CMP materials and their chemical materials, gas chemistries, wafers, filament, phase change memory materials, cost down, reliability, high yield, manufacturability are also in our scope. Innovative materials for sensor and actuator achieving cloud and edge computing are highly welcome.

Reliability & Modeling: papers in all areas of numerical, analytical (including compact/SPICE) and statistical modeling and simulation of electronic, optical or hybrid devices, their interconnect, and 2D / 3D integration; in context of materials, fabrication processes, and devices, e.g. advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport); Mechanical or electro-thermal modeling and simulation; Test structures and methodologies; Front-end and back-end manufacturing processes; 3D integration and wafer-level packaging; Reliability of materials, processes, and devices; Advanced interconnects; ESD, latch-up, soft errors, noise and mismatch behavior, hot carrier effects, bias temperature instabilities, and EMI; defect monitoring and control; manufacturing yield modeling, DFM, analysis, and testing.

Important dates

November 4, 2016:

Initial extended abstract submission deadline – one page text and one page Figure

December 12, 2016: notification of acceptance

January 16, 2017:

Final camera ready 3-page manuscript submission deadline

For more information, please visit the conference website, http://ewh.ieee.org/conf/edtm/2017.

Shuji Ikeda
EDTM ExCom (Japan)
tei Solutions Inc.
Tokyo, Japan

2017 IEEE International Memory Workshop (IMW)

The 9th International Memory Workshop (IMW) will be held at the Hyatt Regency Monterey in California from May 14–17, 2017. The history of the IMW dates back to the NVSMW (Nonvolatile Semiconductor Memory Workshop) which began in 1976 and then later merged with the ICMTD (International Conference on Memory Technology and Design). The IMW is significantly broader in scope than its parent meetings, covering all memory types as well as the co-evolution of memory technology and memory system design. The workshop is focused on advancing innovation in memory technology and provides increased professional development and networking opportunities for attendees while still maintaining a small workshop experience. The IMW is sponsored by the IEEE Electron Devices Society and meets annually in May.

The IMW is the premier international forum for both new and seasoned technologists with diverse technical backgrounds to share and learn about the latest developments in memory technology with the global community. The scope of workshop content ranges from new memory concepts in early research to emerging technologies to the technology drivers currently in volume production. Topics include new and emerging device concepts, technology advancements, scaling and integration, circuit design and reliability, as well as emerging applications. Consistent with the increased importance of memory system architecture and integration, the workshop also includes increasing coverage of the evolving systems in which memories are deployed.

The IMW is the preeminent forum covering the latest developments, innovations, and evolving trends in the memory industry. Highlights from the 2016 workshop included invited talks from renowned industry and research leaders outlining their visions for 3D NAND Moore's law scaling acceleration, breakthroughs enabled by 3D X-point memory, the future of STT MRAM in mobile computing, the outlook for universal memory research, and the future of embedded memory technology in the rapidly expanding IOT market. Typical workshop attendance exceeds 250 attendees and the technical program begins with a full day short course given by renowned experts that provides an excellent professional development opportunity for both new and experienced technologists. The single-track program spans three days and also includes an evening poster session for informal technical discussion with authors as well as a panel discussion with experts weighing in on a current hot topic. The technical program is organized to maximize networking opportunities and facilitate open information exchange among workshop contributors, committee members, and attendees. The program schedule includes ample time dedicated to social events including provided refreshment breaks, a workshop luncheon, and an evening banquet. The workshop is located in the beautiful Monterey Bay area, within close proximity to numerous area attractions and downtown Monterey.

On behalf of the organizing committee, I cordially invite you to participate in the 2017 IMW to continue to advance and/or stay current on both the latest and future innovations in the rapidly evolving memory industry. For additional information, including the call for papers, key dates, abstract submission instructions, registration information, and technical program details, please visit the IMW website for the latest updates: http://www.ewh.ieee.org/soc/eds/imw/. I look forward to seeing you in Monterey this May.

Randy Koval
2017 IMW General Chair
Intel

Society News

Message from President-Elect

Fernando Guarin
President Elect
(2016–2017)

Dear Readers and EDS Members:

It is once again a true honor and privilege to write to you as the EDS President Elect 2016–2017. I will take this opportunity to outline my vision for the direction in which our society should move in the years ahead. We live in interesting times and continue to reap the benefits brought about by the many contributions from EDS members that have shaped society and the world in which we live. Long gone are the days of the predictable path dictated by the traditional scaling of semiconductor devices. It is true that there remain many questions to be answered about the particular embodiment of the electron devices that will dominate future applications in the same manner that Bipolar/CMOS semiconductor devices have done in the past decades. As we set our sights into the future, it is unquestionable that switching devices will provide a path to the future of a vibrant semiconductor industry and will continue to shape our world, enabling solutions to some of the great challenges we face. 1) Feeding and enabling health services for a growing population. 2) Cleaning and preserving our water supplies. 3) Processing the ever growing amounts of information that will grow even more as we embrace the Internet of Things – IoT. 4) Enabling green energy to mitigate climate change. These solutions will be enabled in great measure thanks to the research and contributions of our EDS members in industry and academia throughout the world. The one goal that we must have as our guiding principle in all of our activities is the continued commitment of EDS to the realization of our vision of "Promoting excellence in the field of electron devices for the benefit of humanity." How do we continue to translate this vision into a reality? The central part of the answer is to provide our members with the infrastructure and network to enhance their skills in order to achieve the full potential of their careers. We will continue to impart excellence and leadership in our field by providing a vibrant network of teachers, colleagues and mentors. All with unsurpassed access to the required infrastructure that will serve and support our current and future members in all of the core areas of EDS; publications, conferences, education, awards and chapters all around the globe while we continue to grow our membership and work hard to reach out to young bright minds to replenish and invigorate the future of our society. EDS will continue offering programs that will enhance the skill set of our members at all levels (student, young professional and experienced professional members) providing training and exposure to the research of fellow members in industry and academia. As our Society continues to organize webinars by leading experts from industry and academia in all of our fields of interest. We also provide a solid platform of leading publications, where our members can learn and share the fruits of their research in the field. EDS offers initiatives that will serve our students and young professionals in every corner of the world, offering STEM programs like EDS-ETC that will give them an opportunity to go out to their local environments and share their passion for engineering and keep the pipeline replenished with younger students. Our web content and open access publishing are growing progressively. We are enhancing our support of humanitarian projects enabling our students to form Special Interest Groups in Humanitarian Technology SIGHT. Our society will also encourage and support innovative, creative, and potentially disruptive approaches to the implementation of electron devices while serving the current and future needs of our members. As a closing remark, I would like to request your feedback and ideas on ways to continue improving the value of EDS to our members and to our society.

Fernando Guarin
President Elect (2016–2017)
Global Foundries
East Fishkill, New York, USA
Email: fernando.guarin@ieee.org

Message from Editor-in-Chief

M. K. Radhakrishnan
Editor-in-Chief

Dear EDS Members and Readers,

I have been writing this column for the past 3 years as Editor-in-Chief of the Newsletter. From the very beginning of taking responsibility, and in every issue, I briefly wrote what topics were included and requested reader feedback. This message as well as some of the major changes in the content of the Newsletter was initiated in 2103 with the approval of the EDS leadership team. Major content changes include, an invited technical article explaining any significant technical development related to devices as a lead story written by an expert in a language digestible to all our members; a column of reflections from Young Professionals including an interview with a YP, and messages from the EDS leadership team. Apart from these, we the editorial team tried our best to speed up the Society news and Regional news to reach out to the members as fast as possible, within the publication frequency of the Newsletter. In the meantime, we also opened our Newsletter so that everyone can read irrespective of being an IEEE/EDS member or non-member with an online version available. We wanted to improve the Newsletter with technical briefs and technical content covering half the volume. Target set by me was about six years to develop it as a more versatile technical Newsletter useful to young professionals and students, and now we are only half-way through in our efforts. To my readers, I am afraid whether I will be able to fulfill my vows for the Newsletter as I may have to take a leave soon. However, recently we started getting very positive feedback from readers and I am happy that the efforts are being appreciated by the readers.

This issue of the Newsletter has a technical article on MEMTRONICS written by an expert team, a preview of the upcoming IEDM 2016, an interview of a young professional as the Reflections from YP and reports of a number of EDS mini-colloquia and Distinguished Lectures organized by many Chapters around the globe. These are apart from our usual columns, Society news and announcements.

As mentioned, we are in the process of transformation and to complete it in all respects we need cooperation and timely feedback – both critical and appreciative – from our members and readers. Again, that is why I am repeating the request to provide your candid opinion by e-mail to either: edsnewsletter@ieee.org OR to me radhakrishnan@ieee.org

M. K. Radhakrishnan
Editor-in-Chief, EDS Newsletter
e-mail: radhakrishnan@ieee.org

Message from VP Publications and Products

Hisayo S. Momose
EDS Vice-President of Publications and Products

Dear fellow EDS Members:

It is my great pleasure to write to you as the new Vice President of Publications and Products. For over 30 years, since I started to research transistors in semiconductor area, I have been really encouraged by this global professionals' community, EDS.

Our EDS publications' activities are critical to promote excellence in the field of electron devices. Emerging technologies have been expanding and changing rapidly. We would like to change and be more flexible to meet members' need and provide better service to the community.

Based on the paper download statistics from IEEE Xplore, our flagship journal, the *IEEE Transactions on Electron Devices (T-ED)* has been ranked among the top 10 in all IEEE publications, and our flagship letter, the *IEEE Electron Devices Letter (EDL)* has been top-ranked in the IEEE Letters publications. The submissions to our first open access (OA) journal, the *Journal of Electron Devices Society (J-EDS)* has been increasing year by year since it launched in 2013. We will promote strategically to make J-EDS one of the top-tiered topical OA publications in competing OA publications on device technology.

Last year we welcomed two new EiCs, Giovanni Ghione for T-ED and Tsu-Jae King Liu for EDL by the EiC selections using new EiC Selection and Evaluation Procedures for the EDS journals. We also welcomed Mickael Ostling as a new EiC of J-EDS this September. We will strive further to improve our publications' value for EDS members. We hope researchers report any devices-related subjects in EDS publications as the first consideration.

We need to keep the quality of published papers as high as possible. In addition, to make our publications more attractive and timely, we need to catch new developing areas timely and increase submitted manuscripts in such emerging fields. In order to improve our journals further, your feedback is really appreciated. If you have any suggestions and comments, please let me know by email (h.s.momose@ieee.org) or Ms. Marlene James, Supervisor EDS Publications (m.james@ieee.org).

Sincerely,

Hisayo S. Momose
EDS Vice-President of Publications and Products
Yokohama National University
Yokohama, Japan

EDS Membership Fee Subsidy Program (MFSP)

Applications Now Being Accepted for 2017 EDS Membership Fee Subsidy Program

Tian-Ling Ren
EDS Vice-President of Membership and Services

Our society continually works to increase the value of EDS membership and our colleagues enjoy an incredible array of free and deeply-discounted, members-only benefits. One EDS initiative to encourage newcomers and assist current members is the **EDS Membership Fee Subsidy Program** (MFSP). This program offers the generous incentive of one year complimentary IEEE and EDS memberships to help launch new chapters or enable existing ones, in low income geographical areas to grow their memberships.

This special offer is available to students and to those professionals who meet the eligibility requirements.

To complement our Society program, we are encouraging members in eligible countries to try IEEE e-Membership (an electronic membership option with reduced fees). Please visit the IEEE website for more details on e-Membership: http://www.ieee.org/membership_services/membership/join/emember.html.

The EDS Membership Fee Subsidy Program policy is as follows:

- EDS will cover the cost of a full year of IEEE and EDS membership for up to 15 new or current members per chapter, provided the existing members have not received MFSP benefits in the past.
- **Five** of the fifteen members each year must be new IEEE/EDS members.
- New and renewing members must apply through their local chapter. Current elected officials of eligible chapters will receive instructions from the EDS Executive Office.
- Chapter Chairs must verify member's eligibility according to IEEE income guidelines. A complete list of special circumstances eligible for reduced IEEE membership dues can be found on the IEEE website, at http://www.ieee.org/membership_services/membership/cost/special_circumstances.html.

Please visit the EDS website for more information on the EDS Membership Fee Subsidy Program: http://eds.ieee.org/mfsp.html. Any questions should be directed to Joyce Lombardini (j.lombardini@ieee.org), EDS Membership Administrator.

Tian-Ling Ren
EDS Vice-President of Membership and Services
Tsinghua University
Beijing, China

EDS VLSI Technology and Circuits Technical Committee

On June 15, 2016, the IEEE EDS *VLSI Technology and Circuits* Technical Committee (TC) met in Honolulu, Hawaii, USA during the 2016 Symposium on VLSI Technology, held June 13th–16th.

The mission of the VLSI Technology and Circuits TC's is to identify new technical trends, help foster new technical concepts, and serve the emerging needs of the Electron Devices and Solid-State Circuits communities in VLSI. The committee members include many well recognized technical experts representing a wide spectrum of technical mastery in VLSI devices, technology, and circuits.

In pursuing the objective to identify new and relevant areas of interest to the Electron Devices and Solid-State Circuits communities, the committee recommends any or all of the following based on the nature of the areas:

1. Initiate topical workshops of current interest (attached to existing conferences or incorporated in new ones)
2. Promote special issues for major publications (e.g., T-ED, J-EDS)
3. Sponsor panel session topics, invited talks and special sessions for major conferences

The topics discussed during the June 15, 2016 meeting included: Committee membership and regional participation, Sub-Committee roles and responsibilities and EDTM support.

Based on strong manufacturing technologies, Asia has the potential to take the initiative for system integration. Deep-diving discussions among societies on material, process and devices are essential to accelerate manufacturing innovations through this conference.

The Inaugural EDTM – Electron Devices Technology and Manufacturing will be a full three-day conference to be held at Toyama International Conference Center, Japan, from February 28th to March 2nd, 2017, fully sponsored by the IEEE Electron Devices Society (EDS). As semiconductor technology scaling challenges continue to grow, the industry must increase collaborative efforts to overcome them. EDTM serves as a forum for the electron devices community to collaborate on topics ranging from devices, materials, and tools, to create new and innovative technologies.

For further details please contact Dr. Reza Arghavani (Reza.Arghavani@lamresearch.com), Conferences/Workshops Subcommittee Chair, or Dr. Shu Ikeda (shu.ikeda@tei-solutions.com) Committee Chair.

Reza Arghavani
EDS VLSI TC Committee Member
Lam Research Corporation
Fremont, CA, USA

IEEE/OSA Journal of Display Technology (JDT)

Dear EDS Members:

The *IEEE/OSA Journal of Display Technology (JDT)* will cease publication with its October-December 2016 issue, due to be published early December 2016.This publication, along with its archived content, will continue to be accessible to EDS members on the *IEEE Xplore* platform as part of your membership benefits. The IEEE has a number of highly-cited journals that will be accepting papers which cover appropriate segments of the IEEE/OSA JDT's focus area. Within the Electron Devices Society (EDS), we hope you consider one of our following journals for your manuscript submissions:

1) *IEEE Journal of the Electron Devices Society* (J-EDS), an Open Access (OA) publication;
2) *IEEE Transactions on Electron Devices* (T-ED);
3) *IEEE Electron Device Letters* (EDL).

Sincerely,

Hisayo S. Momose
EDS Vice-President of Publications and Products
Yokohama National University
Yokohama, Japan

Letters to the Editor

Dear Editor,

I'd like to offer my praise for an excellent article! As a semiconductor-physics-challenged electrical engineer, it is quite an accomplishment for Mayank Shrivastava and V. Ramgopal Rao to 1) keep my attention for a full article and 2) get me to understand most of the physics behind the devices. I found their Technical Brief "Tunnel Field Effect Transistors: Past, Present, and Future" in the July 2016 issue fascinating and easy to read. I thoroughly enjoyed the article.

Jim (James) Ford
Principal Engineer

MK, I always enjoy perusing the newsletter, helps keep me in touch and very much appreciate your diligence with the newsletter.

Randy Rannow
Apichip.com
Culver City, California

Volunteers Needed for IEEE Humanitarian Programs

In recent years, IEEE has placed great emphasis on Humanitarian Technology Activities as part of its strategic efforts to advance technology for the good of humanity. A program called Special Interest Group on Humanitarian Technology (SIGHT) was created to further these efforts.

EDS members interested in devoting their time and talents to an IEEE humanitarian project will find that there are many opportunities.

IEEE SIGHT
Special Interest Group on Humanitarian Technology

We encourage current EDS chapters to form a SIGHT group and qualify for the $250 seed funding.

Should you submit a proposal to start a new SIGHT group and participate in any of the IEEE humanitarian programs, please make sure to indicate the Electron Devices Society as your Operating Unit (OU).

For more details on this program, visit the IEEE SIGHT webpage: http://www.ieee.org/special_interest_group_on_humanitarian_technology.html.

Call for Nominations for IEEE Electron Devices Society Newsletter Editor-in-Chief

Since July 1994, the IEEE Electron Devices Society (EDS) Newsletter has been a flagship publication of the IEEE Electron Devices Society (EDS). The EDS Newsletter, published quarterly, covers regional and chapter activities, technical meetings, awards and other news and initiatives of the society. The EDS Newsletter publishes technical articles and reports from experts providing a general outline or standing in the respective areas of field of interest of EDS to our readers. Two sections on Young Professionals (YP) and Chapters News are included to encourage YP participation and highlight the activities of vibrant Chapters. Messages from the EDS Officers (President, President-Elect, Secretary, Treasurer) and VPs appear in each issue to highlight the current and future evolutions of EDS.

We invite nominations for the position of Editor-in-Chief (EiC) for the EDS Newsletter for a 3-year term beginning in **January of 2017**.

The EiC's duties include supervising the operations of the EDS Newsletter with the assistance of the EDS publications staff and collaboration of Regional Editors; monitoring the quality and timeliness of publications in its paper and e-formats; editing, reviewing and proof reading all articles published in the EDS Newsletter; inviting Technical Articles from experts, messages of EDS Officers and VPs, and articles from Vibrant Chapters; conducting interviews of Young Professionals; recommending Regional Editors to serve across the scope of the journal; leading development to strengthen the Newsletter; reporting to the EDS Newsletter Oversight Committee twice per year and take up actions for the next period.

Criteria for the Nominees:

- Ability and motivation to spend sufficient time on the job;
- Demonstrated technical leadership in EDS field-of-interest and commitment to volunteer;
- Formal support from the institution for which the nominee works (waived if self-employed);
- Has served or currently is serving as editor at the Regional level or as experienced editor at other EDS publications.
- Be a member of EDS and willing to support EDS procedures and policies;
- Commitment to guiding the publication according to this Call for Nominations;
- In addition, the EIC must demonstrate a willingness to work collaboratively with internal and external stakeholders so to ensure the advancement of the society's vision and mission as well as the technical and fiscal health of the Newsletter.

Requirement for Nominations:

- A brief IEEE-style biography (up to 250 words) of the nominee;
- A complete CV and list-of-publications of the nominee;
- A brief statement from the nominator on nominee's qualification and how the nominee meets the criteria listed above;
- A letter from nominee's employer indicating support for the EiC activity;
- Endorsement from two EDS members on the nomination;
- Optionally, a statement (up to 500 words) from the nominee on his/her vision for the journal.

Please email the nomination materials to: Marlene James (m.james@ieee.org) no later than October 31, 2016.

Simon Deleonibus
Secretary
IEEE Electron Devices Society

2015 EDS Paul Rappaport Award

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. Every year, the Society confers its prestigious Paul Rappaport Award to the best paper published in the *IEEE Transactions on Electron Devices*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The winning paper was selected from over 600 articles that were published in 2015. The winning paper is entitled *"Noise-Induced Resistance Broadening in Resistive Switching Memory—Part I: Intrinsic Cell Behavior / Part II: Array Statistics."* This paper was published in the November 2015 issue of the *IEEE Transactions on Electron Devices*, and was authored by Stefano Ambrogio, Simone Balatti, Vincent McCaffrey, Daniel C. Wang and Daniele Ielmini.

The award will be presented at the plenary session of the IEEE International Electron Devices Meeting to be held on December 5, 2016, in San Francisco, California. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of the authors follow.

Stefano Ambrogio received the M.S. and Ph.D. degrees in Electrical Engineering from Politecnico di Milano, Italy, in 2012 and 2016. His main research interests are electrical characterization, modeling and neuromorphic computing of resistive switching memories (RRAM, PCM). He is first author of nine papers on peer-reviewed journals and has given talks in various international conferences (IEDM, VLSI, and MRS).

Simone Balatti received the B.S., M.S., and Ph.D. degrees from the Politecnico di Milano, Milan, Italy, in 2009, 2011, and 2015, respectively, all in electrical engineering. He is currently a Device Engineer with Intermolecular, Inc., San Jose, CA, USA. His current research is focused on the study of novel devices for memory applications.

Daniele Ielmini, Ph.D., is an Associate Professor at Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano. He conducts research on emerging nanodevices, such as phase change memory (PCM) and resistive switching memory (RRAM). He published more than 250 papers in peer-reviewed journals and international conferences. He received the Intel Outstanding Researcher Award in 2013 and the ERC Consolidator Grant in 2014. He is a Senior Member of the IEEE.

Vincent McCaffrey received the BS degree in electronic engineering from University College, Dublin, Ireland, in 1981. Since then, he has worked in the semiconductor industry in the fields of technology reliability and product engineering for FPGA's and non-volatile memories. He is currently employed at Maxim Integrated, working on the characterization, reliability, and qualification of power management ICs.

Daniel C. Wang was born in Tainan, Taiwan, in 1965. He received his B.S. degree in electrical and computer engineering from National Central University, Taiwan in 1988, and the M.S. and Ph.D. degrees in electrical engineering from University of Florida, USA in 1992 and 1996, respectively.

He is a Senior Member of Technical Staff at Adesto Technologies. His current research interests include nonvolatile memory operation and device reliability with a special focus on resistive-switching memory and conductive-bridge memory.

Hisayo S. Momose
EDS Vice-President of Publications and Products
Yokohama National University
Yokohama, Japan

2015 EDS George E. Smith Award

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. The George E. Smith Award was established in 2002 to recognize the best paper appearing in a fast turnaround archival publication of EDS, targeted to the *IEEE Electron Device Letters*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The paper winning the 2015 George E. Smith Award was selected from 400 articles that were published in 2015. The paper is entitled, *"First Demonstration of Amplification at 1 THz Using 25 nm InP High Electron Mobility Transistor Process."* This paper appeared in the February 2015 issue of the *IEEE Electron Device Letters* and was authored by Xiaobing Mei, Wayne Yoshida, Mike Lange, Jane Lee, Joe Zhou, PoHsin Liu, Kevin Leong, Alex Zamora, Jose Padilla, Stephen Sarkozy, Richard Lai, and William R. Deal.

The award will be presented at the plenary session of the IEEE International Electron Devices Meeting to be held on December 5, 2016, in San Francisco, California. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of the authors follow.

Xiaobing Mei received his Ph.D. degree in electrical engineering from University of California, San Diego in 1997. He is a Senior Staff Engineer at Northrop Grumman's Micro Electronics Center, leading advanced InP HEMT technology development.

Wayne Yoshida received a B.S. in Chemical Engineering from the California Institute of Technology and Ph.D. in Chemical Engineering from UCLA. He has worked for Northrop Grumman in the field of advanced lithography since 2003, and currently serves as Technical Lead for the Electron Beam Lithography group in the Microelectronics Process Department.

Michael D. Lange received his Ph.D. from the University of Illinois at Chicago in 1993. From 1986 to the present, he has worked in R&D of compound semiconductor materials by MBE. In 2002, he joined Northrop Grumman Aerospace Systems for R&D of compound semiconductor materials and structures for transistor circuits.

Jane Lee worked as a semiconductor process engineer in Northrop Grumman for over 30 years. Jane received a Master of Science degree in metallurgical engineering from Ohio State University, a Master of Science degree in chemistry from University of Notre Dame and a Bachelor of Science degree in chemistry from National Taiwan University.

Joe Zhou received his B. S degree in Metallurgical engineering from Northeast University of China, in 1984, and his Ph.D. degree in metallurgical engineering from University of Missouri in 1996. He was a Staff Engineer at Northrop Grumman's Micro Electronics Center, leading advanced InP HEMT technology in backside process development.

Po-Hsin Liu was the research and production lead of the advanced E-beam lithography group at Northrop Grumman Aerospace Systems for over 30 years. He has recently retired in 2016 after 36 years of distinguished service at Northrop Grumman.

Kevin Leong received a B.S. degree from University of Hawaii and Ph.D. degree from UCLA, both in electrical engineering. From 2004 to 2007, he was a postdoctoral researcher at UCLA. Currently, he is a staff engineer at NGAS where he is involved in high frequency MMIC and package design.

Alexis Zamora earned his B.S. and M.S. degrees in electrical engineering from the University of Hawaii at Manoa in 2008 and 2010, respectively. Since 2011 he was been a staff engineer at Northrop Grumman Aerospace Systems, Redondo Beach, CA, where he predominantly does MMIC design on various III–V technologies. His main area of interest is InP-HEMT-based high frequency electronics.

Jose Padilla is the Transmitters & Receivers section manager for the

Radio Frequency & Mixed Signal department at Northrop Grumman Aerospace Systems. He has more than 20 years of experience developing advanced technologies and products in the RF electronics and photonics fields in the aerospace, defense, and commercial industries.

Stephen Sarkozy received the Ph.D. Degree in natural science (Semiconductor Physics) at the Cavendish Laboratory, University of Cambridge in 2008 as a Northrop Grumman Space Technology Doctoral Fellow. He is currently a Northrop Grumman Program Manager involved in advanced technologies and systems for academic, commercial, and military applications.

Richard Lai is a Northrop Grumman Aerospace System Technical Fellow researching and developing advanced GaAs and InP-based HEMT and MMIC RF technologies and products to achieve the lowest noise and highest frequency devices and circuits. He is an IEEE Fellow elected in 2010.

William Deal is a Distinguished Engineer with Northrop Grumman's RF&MS Department, where he is responsible developing Millimeter to Sub-Millimeter Wave integrated circuits and hardware. Research interests include integrated circuit design, device modeling and Terahertz Electronics. He is associate editor for the IEEE MWCL and IEEE TTST.

Hisayo S. Momose
EDS Vice-President of Publications and Products
Yokohama National University
Yokohama, Japan

IEEE EDS William R. Cherry Award Call for Nominations

The IEEE Electron Devices Society invites the submission of nominations for the 2017 William R. Cherry Award.

This award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry award was instituted in l980, shortly after his death. The purpose of the award is to recognize an individual engineer or scientist who devoted a part of their professional life to the advancement of the science and technology of photovoltaic energy conversion.

The award consists of a plaque, monetary award, recognition at the PVSC Opening Ceremony and a dedicated Cherry Award Talk during the Opening Ceremony. In addition, a reception is held in honor of the Cherry Award winner during the PVSC.

Nominate:
William R. Cherry Award on-line nomination form:
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Electron Devices Society Members Named Recipients of 2016 IEEE Medals

Two EDS members were named 2016 IEEE Medal award winners. Please be sure to visit IEEE TV at http://ieeetv.ieee.org/ to view the award presentations and acceptance speeches.

2016 IEEE Jun-Ichi Nishizawa Medal

MASAYOSHI ESASHI of Tohoku University has been named the recipient of the 2016 IEEE Jun-Ichi Nishizawa Medal. His citation states, *"For pioneering contributions to micro-electro-mechanical systems (MEMS), and their uses in automobiles, cellular phones, industrial equipment, and medical devices."*

Masayoshi Esashi has been a pioneering force of micro-electro-mechanical systems (MEMS) technology for over 40 years, developing and bringing to market the tiny sensors and actuators that provide advanced functionalities in today's automobiles, cellular phones, industrial equipment, and medical devices. Esashi's key contributions to biomedical microsensors began in the 1970s, where his work on an ion-sensitive field-effect transistor (ISFET) led to the development of medical catheters for in-vivo pH and PCO2 monitoring. During the 1980s, Esashi developed many MEMS and integrated circuit (IC) devices including a servo-type accelerometer, networked tactile sensor, multifreedom active catheter, and a monolithically integrated capacitive pressure sensor that was commercialized by Toyoda Machine Works. The microfluidic system developed by Esashi during the 1990s, which featured microchannels, flow sensors, valves, and pumps on a silicon wafer, provided the foundation for the micro total analysis system/lab-on-a-chip technologies of today. To provide the often-lacking tools needed for continued innovation of MEMS-based devices, Esashi used his IC research and development experience to help develop etchers, deposition machines, and special lithography and evaluation tools. His development of an ion-reactive etcher enabled the fabrication of deep trenches in silicon, which was critical to the commercialization of inertial sensors now used in over 1 million automobiles for active safety control. Another hallmark of Esashi's career has been his belief in "open innovation" collaboration. He established the Micro System Integration Center where companies can work together to advance MEMS technologies. This has resulted in wafer-level-based hetero-integrated devices such as piezoelectric MEMS switches for mobile phones, monolithic tunable filters for cognitive radios, MEMS-on-IC networked tactile sensors for human-friendly robots, and massively arrayed electron beam emitters for maskless high-speed nanolithography.

An IEEE Member and recipient of the Medal with Purple Ribbon from the government of Japan, Esashi is a professor with Tohoku University, Sendai, Miyagi, Japan.

2016 IEEE Robert N. Noyce Medal

TAKUO SUGANO of the University of Tokyo has been named the recipient of the 2016 IEEE Robert N. Noyce Medal. His citation states, *"For contributions to and leadership in the research and development of the science and technology of semiconductor devices."*

Takuo Sugano has dedicated his career to strengthening the understanding of semiconductor materials to enable progress in developing advanced silicon-based electronic devices and the continued growth of the industry. During the 1960s, he tackled instability issues in silicon metal-oxide-field-effect-transistors (MOSFETs) caused by sodium contamination. Using radio-activation analysis, Sugano demonstrated the physical mechanism of prevention of sodium ions from moving in the dielectric, leading to more stability and enabling more reliable and high-performance MOSFETs. Assuming that chemical bonds between silicon and oxygen or silicon at silicon dioxide-silicon interfaces are stretched, he also proposed a novel model on the origin of the U-shaped energy distribution of density of trap state at silicon dioxide-silicon interfaces. His work on electron transport in the silicon inversion layer highlighted the effect of surface quantization of carriers in MOSFET channels at room temperature to improve the dynamic characteristics of silicon MOSFETs. The resulting improvement in performance helped move the commercial application of silicon MOSFETs beyond personal calculators. To further improve MOSFET reliability, Sugano then focused his efforts on electron and hole trapping in silicon dioxide films that were thermally grown in an ultra-dry or conventional oxidizing atmosphere on the surface of silicon substrates and the generation of interface trap states by electron or hole injection. Also important to increasing the understanding of

semiconductor materials was Sugano's role in establishment of a class-100 clean room in 1975 at the University of Tokyo at a time when clean rooms were not popular at universities. Sugano has also made pioneering contributions to III–V semiconductors, superconducting (Josephson junction) devices, and single-electron transistors. He developed an anodic oxidation process for III/V compound semiconductors in inductively coupled plasma and demonstrated its usefulness for fabricating gallium arsenide insulated-gate FETs. He also has made important contributions to plasma processes for fabrication of silicon large scale integrated circuits, including plasma etching, plasma cleaning, and plasma oxidation.

An IEEE Life Fellow and recipient of the Person of Cultural Merit award (2006) from the government of Japan, Sugano is a Professor Emeritus with the University of Tokyo, Tokyo, Japan.

Albert Wang
EDS Awards Chair
University of California
Riverside, CA, USA

EDS Members Recently Elected to IEEE Senior Member Grade

Srimanta Baishya
Can Bayram
Cornell Chun
Xiangyi Guo
Neena Gupta
Bruce Hecht
John Hutson
Russ Jones
Chin Seng Khor
Peter Manos
Jesus Mejia Silva
N. Mohankumar
Marcos Ramos Blume
Mayank Shrivastava
Arun Singh
Jorge Tejada-Polo
Thomas Vandervelde
John Wilson
Dong-Sing Wuu

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status. For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application after signing in with your IEEE account: https://www.ieee.org/membership_services/membership/senior/application/index.html

Please remember to designate the Electron Devices Society as your nominating entity!

2014–2015 EDS Region 9 Outstanding Student Paper Award

The prestigious 2014–2015 EDS Region 9 Outstanding Student Paper Award was presented by 2016–2017 EDS President-Elect Fernando Guarin to Fabián Zárate-Rincón at the SBMICRO 2016 conference in Belo Horizonte, Brazil, on August 30th.

Announcement of the 2016 EDS Ph.D. Student Fellowship Winners

Carmen M. Lilley
EDS Student Fellowship Committee Chair

The Electron Devices Society Ph. D. Student Fellowship Program was designed to promote, recognize, and support Ph.D. level study and research within the Electron Devices Society's field of interest.

EDS proudly announces three EDS Ph.D. Student Fellowship winners for 2016: **Jiahao Kang** – University of California, California, USA, **Hagyoul Bae** – Korea Advanced Institute of Science and Technology, Republic of Korea, **Chao-Yang Chen** – University of Toronto, Leuven, Belgium. Brief biographies of the recipients appear below. Detailed articles about each Ph.D. Student Fellowship winner and their work will appear in forthcoming issues of the EDS Newsletter.

Jiahao Kang joined the UCSB *Nanoelectronics Research Lab* of Prof. Kaustav Banerjee, in Fall 2010 as a MS/Ph.D. student upon completing his BE degree in microelectronics from Tsinghua University, Beijing, China. Mr. Kang's research is at the very core of developing next-generation ultra-energy-efficient electronics and exploited the unique physics of graphene and beyond-graphene two-dimensional electronic materials. His work spanned fundamental materials physics, including the physics of contacts and interfaces, to device design and finally to experimental demonstration of applications uniquely enabled by these materials. His research contributions are chronicled in around 40 papers in leading IEEE conferences and journals including IEDM, TED and EDL, as well as in Nature, Nature Materials, Nature Nanotechnology, Nano Letters, ACS Nano, Physics Review X and Applied Physics Letters.

Hagyoul Bae received the B.S. and M.S. degrees in Electrical Engineering from Kookmin University, Seoul Korea. He is currently pursuing the Ph.D. degree in Electrical Engineering at Korea Advanced Institute of Science Technology (KAIST) under the supervision of Prof. Yang-Kyu Choi. Hagyoul Bae has published 39 research articles in major peer-reviewed scientific

journals (34) and international conferences (5). His current research interests include fabrication, modeling, and characterization of 2D-material FET (MoS_2 and graphene), organic/inorganic based resistive random access memory (RRAM), physically transient memory, wearable electronics, Ge based nanostructured devices, amorphous oxide semiconductor thin-film transistors (AOS TFTs), and high mobility SiGe MOSFET.

Chao-Yang (Michael) Chen received his B.ASc. and M.Sc. in Engineering Science and Material Science Engineering in 2010 and 2013, respectively both from University of Toronto, Ontario, Canada. Currently, he is working toward the Ph.D. degree at imec/Katholieke Universiteit Leuven, Belgium.

Carmen M. Lilley
EDS Student Fellowship
Committee Chair
University of Illinois at Chicago
Chicago, IL, USA

Announcement of the 2016 EDS Masters Student Fellowship Winners

Carmen M. Lilley
EDS Student Fellowship Committee Chair

The Electron Devices Society Masters Student Fellowship Program was designed to promote, recognize, and support Masters level study and research within the Electron Devices Society's field of interest.

EDS proudly announces the winners of the 2016 EDS Masters Student Fellowship.

Haitong Li received the B.S. degree in microelectronics from Peking University, Beijing, China, in 2015. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, Stanford University, Stanford, California, USA, supervised by Prof. H.-S. Philip Wong. His current research interests include brain-inspired computing with emerging memories. Haitong has published more than 25 papers appearing in Scientific Reports, *IEEE EDL, IEEE T-ED,* and top-tier conferences including VLSI (nominated for 2016 Best Student Paper Award), IEDM, and DATE. He serves as an active reviewer for *IEEE EDL* (listed in "2015 Golden Reviewers"), *IEEE T-ED*, Scientific Reports, APL, *IEEE T-CAD, and IEEE T-NANO*.

Yi-Pei Tsai was born in Taiwan in 1992. She received the M.S. degree in electronics engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2016. Her major is solid state physics of electronic engineering and current research interest is plasma induced damage recorders in advanced CMOS FinFET processes. The On-chip In situ recorders in FinFET technologies can identify the polarity and sources of plasma stress across the wafer. These excellent research works were published in the famous IEEE conference, International Electron Devices Meeting (IEDM 2015) and in *IEEE Transactions on Electron Devices (TED)* in 2016.

Carmen Lilley
EDS Student Fellowship
Committee Chair
University of Illinois at Chicago
Chicago, IL, USA

Young Professionals

Reflections from EDS Young Professionals

Camilo Velez Cuervo

The EDS Newsletter would like to hear from IEEE Young Professionals who as EDS members would like to share their thoughts and experiences with other members through the Newsletter column in an interview format. To encourage this discussion forum, the *Editor-in-Chief of the EDS Newsletter* has set up a few questions for which the YP may answer in his/her own way, as necessary to substantiate the views. The YP's views will be shared in the Newsletter along with his/her credentials.

MKR: As a young professional, why do you consider the membership in IEEE and especially in EDS is important?

Camilo: The importance of being a member to IEEE and EDS can be summarized in "networking".
That was a concept I didn't understand when I was an undergrad. To be honest, I thought that was some political process for very important and rich people (like lobbyist) meeting in fancy clubs and that I would need to be important to be part of that network. But EDS proved me wrong. Networking at EDS is as simple as being yourself and continue working in your own field. People at EDS really care for helping others in the field without seeking retribution. The beauty of EDS is the members that genuinely want to contribute by reaching their hands to the youngest and showing them the path to their future careers. In my case, my professors were members of EDS and they invited other friends and professors to conferences in my city. I attended one of those conferences and met one of those professors who ended up inviting me to work in his lab and to join the Ph.D. program. Networking at EDS is as simple as gossiping and following the clues that other members give you. That is why EDS is so important to me.

MKR: What was the specific temptation, if any, which encouraged you to join the largest professional organization in the globe at first, and to select EDS as your favorite Society?

Camilo: To be honest, the first temptation was obtaining discounts to participate in conferences. But the real motivation was to follow the example of my professors. I discovered how they created their own networks just as simple as making friends at those conferences and understanding how their research and jobs are related. The fascination of attending a conference with people from different countries and discovering new ideas to implement in your own work is enlightening. And knowing that the common denominator is our organization is even better. And EDS is my favorite because it feels like home, like being surrounding by old friends. As a researcher you probably will join many other societies related with other research fields, but I found friends at EDS that keep helping others through years' and countries and that inspires me to do my best.

MKR: As a Professional, what are your interests which coincides with EDS activities and your own technical field? How does your professional life blend with the services you perform as an EDS member/volunteer?

Camilo: I'm a young researcher in micro-nano fabrication and magnetic materials and I try to attend as many webinars and Mini-Colloquia from EDS as possible. I think they are amazing spaces for updating yourself on the state of the art and interacting with distinguished researchers in our field. On the other hand, I tend to give talks and present my work on classes and events at my EDS friend's universities even through Skype. By keeping communication channels open with other members of the society I try to keep some research projects going on at my own country (Colombia), meanwhile I learn new techniques and skills in the USA. And, as I said earlier, keeping the gossip going: as soon as I know about a research opportunity, a friend that needs a new student or an open position, I send the information to my colleges.

MKR: What are your views about EDS membership and its paybacks? Whether the EDS membership stimulated you at any time in your career growth? If so how?

Camilo: I feel stimulated by people and their work. EDS is simple: a group of very talented people that always will stimulate you professionally. You will find at EDS, people that will encourage you all the time. That in a phone call after a couple years of not talking to you, they will ask you if you continue working in a particular field; will ask you if you are studying what you studied a long time ago and challenging you to remain in the field. This stimulation is very particular at EDS because they will throw at you real opportunities; this is real people interacting and helping and not a work placement

advertising service. This is genuine care for helping you and motivating you to pursue your own dreams.

MKR: As a YP, how do you consider the ED Society as a focused professional group? What are the changes or developments you would like to see in evolving this professional body as a group devoted to the humanity and its causes?

Camilo: I do. I think it's so focused that sometimes we forget that we can also help to solve less technically challenging problems. I envision a society that will "use" their members more to help other people, to teach more, for example. I would like to receive more phone calls from the society inviting me to volunteer at local events to help solve community problems.

MKR: As an EDS Young Professional and a young researcher in the field, how do you consider the prospects of scientific research in this field for the progress of Humanity as a whole? Also, in your opinion in what possible ways can the young researchers and professionals around the globe contribute to the development of a peaceful, global human society?

Camilo: It is clear for me that the world is living now in the era of the Internet of Things (IoT) and this is a very nurturing environment for innovation and research in new devices (such as sensors) that enhance the human experience and "digitalize" every interaction with the environment. I believe EDS is a cornerstone in this new era because we should be the never-ending source of new ideas and new solutions to problems that probably we don't even know about yet. But our contributions can also be as simple as to teach a kid how to code, or even teach somebody how to interpret the electricity bill. It is never too soon to start sharing your knowledge to the world and sometimes solving important problems for a community do not require a fancy laboratory, complicated equipment or the highest academic degree, the first step is always to care and work hard to understand the problem.

MKR: What are your specific suggestions and recommendations for those young professionals who may aspire to join EDS?

Camilo: Don't hesitate. Just do it. Join EDS now. Start building your network as early as possible. When thinking about networking, think about planting a tree and please remember and apply the Chinese proverb: "The best time to plant a tree was 20 years ago. The second best time is now."

***Camilo Velez** is a Ph.D. candidate at University of Florida, with a Master of Science, Master of Engineering and a B.S. in Electronic Engineering. He is working on magnetic micro-nano systems and experience on microfluidics, MEMs, III-V semiconductors and VLSI. Camilo worked at SIEMENS Healthcare Diagnostics and is the cofounder of the startup Real NanoMicro.*

EDS-ETC Programs

EDS-ETC Takes Root in Sugar Land

—by Doug Verret

Among other things Texas is known for tumbleweeds and prickly pear cacti. This winter and spring, however, it is beginning to be known for its innovation in STEM education in East Texas. A collaboration has developed including engineers from Texas Instruments Inc, electrical engineering students from Rice University and educators in Fort Bend County. The tri-fold goal of this partnership is to encourage K-12 students to consider careers in STEM (Science, Technology, Engineering and Math) by conducting fun electronics experiments with them; establishing connections between teachers and engineers; and challenging them to think critically and to be inventive problem-solvers. This is all done under the aegis of the well-known EDS-ETC program.

Just in the month of March this year, engineers from Texas Instruments conducted experiments with advanced placement physics classes at Kempner High School. In addition Rice University graduate student Chance Tarver and Doug Verret, a member of the EDS BoG, conducted experiments with physics students at Elkins HS. This was followed by experiments with all the physics classes at George Bush HS conducted by Doug. Lastly, Chance Tarver, Rice undergraduate Jorge Quintero, Doug and two students from Dulles HS explored circuit concepts with 4th and 5th graders at Rita Drabek Elementary School. In May were visits to more physics classes at Kempner HS and the Lake View Elementary School Math Club (4th and 5th graders). The uptake of this program in Sugar Land has been explosive.

Students at Kempner HS constructed circuits using Elenco Snap Circuits® whereby they observed the effect of resistance and capacitance on charge/discharge times as displayed by the varying intensity of an LED. The students were then challenged to design their own circuit with a given time constant. Students at Bush and Elkins HS constructed circuits that displayed the characteristics of OR, AND and NOR gates by

Pictured are (front row, from left) - Shiou Huang, TI engineer; Ashwini Athalye, TI engineer; and Kelly Bird, Kempner High School Physics teacher; (back row, from left) Timothy Harvey, TI engineer; Douglas Verret, EDS representative, and John Nafziger, TI engineer

Dr. Douglas Verret is helping Kempner students trace the current flow in a circuit. Pictured are James Fields (left), Qianting Lin (center), and Dr. Verret (right)

Rita Drabek teacher Katherine Saludis working with students using Snap Circuits

Pictured are (back row, from left) Jorge Quintero, Rice University undergraduate; Douglas Verret, EDS member; and Hasham Dhakwala, Dulles High School student. (Front row, from left) Katherine Saludis, Drabek Elementary School teacher; Smit Shah, Dulles High School student; and Chance Tarver, Rice University graduate student

using switches as inputs and an LED as an output. They were then challenged to construct their own circuit when given a truth table (for a NAND gate) of Boolean variables. They were also asked to build a circuit demonstrating a tri-input NAND gate and record its corresponding truth table. Students were also shown de-capped integrated circuits to illustrate the miniaturization achieved by modern electronics. Incredible as it may seem, in the state science curriculum there is no coverage of digital electronics. In many cases then, this will be the only exposure of Fort Bend students to digital circuit concepts.

To date several hundred students have been involved in electronic circuit experiments with engineers since 2014. Requests from teachers continue to increase and may not be able to be supported with currently available volunteer engineers. It is anticipated that undergraduate electrical engineering students from the University of Houston (two campuses) will join the program in the coming year. Even though we are not likely to replace tumbleweeds or cacti as items of renown, our Society has certainly planted some seeds in Sugar Land and the education cultivators there are exuberant. That is something for which the Society can be proud.

Talent Training Program Empowered by IEEE Electron Devices Society

—by Mansun Chan, EDS Education Committee Chair

In addition to promoting activities through the EDS-ETC program, the Education Committee of the Electron Devices Society has actively collaborated and empowered individual efforts to promote engineering activities to the next generation of the society. On July 18, 2016, EDS provided support to a Talent Training Program organized by Dr. Shangqi Yang, Founder of Syltechi Embedded System Design LLC, at a community center in San Diego, California, USA. The program consisted of four 1.5 hour classes where students were asked to assemble electronics and mechanical components with an arduino board to form a remote control vehicle. Based on the given instructions, the students setup connection between a mobile phone and vehicle to pick up various sensor signals along the course of travel. The program was attended by 9 students with the youngest just completing the 5th grade. Together with 3 parent helpers, it helps to introduce the fun of engineering projects not only to the children, but also to the family.

After the training, the students were given a certificate of participation, issued by the Education Committee of IEEE EDS and were encouraged to participate and help in other activities organized by IEEE and EDS in the near future.

Students assembling the electronic and mechanical components to construct a remote control vehicle

Chapter Organizes Electronic Experience Training Class for Future Engineers

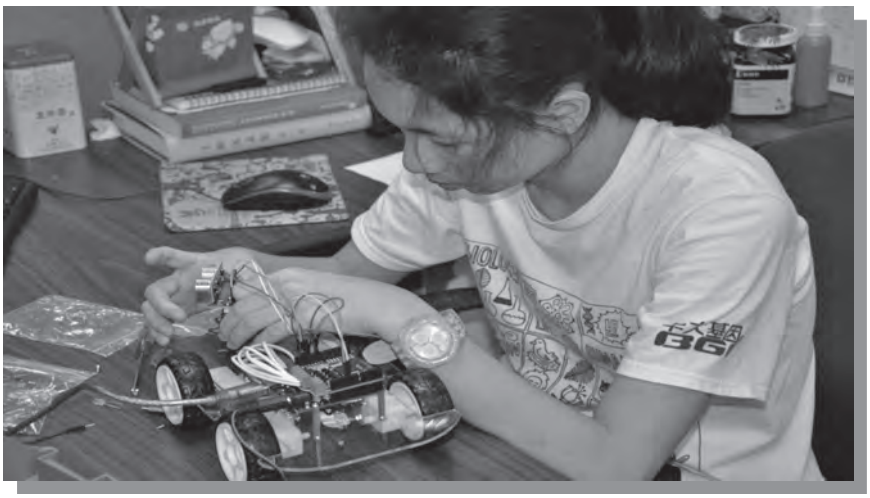
—by Xinnan Lin, Chair of IEEE Beijing Section ED/SSC Shenzhen Joint Chapter

The ED/SSC Shenzhen Chapter held the first training program for secondary school students on the application of electronic devices and circuits. The material was prepared by Dr. Shengqi Yang, Adjunct Professor of Beijing University of Technology and Prof. Xinnan Lin, Associate Professor of Peking University Shenzhen Graduate and IEEE ED/SSC Shenzhen Chapter Chair in collaboration with Prof. Mansun Chan, IEEE Education Committee Chair. The training program was initiated with a brief introduction by Prof. Lin on the organization of IEEE and the Electron

Participants of the talent training program with Dr. Shangqi Yang (middle), the course organizer

A competition between different groups to accomplish a given task

Prof. Xinnan Lin, Chapter Chair (second left, standing), students and helpers



A student constructing an autonomous vehicle

Devices Society on July 25, 2016. During the 5-day event, the students were first introduced to the basic concepts of electronic components, application of sensors and electronic control with microprocessor. In the second half of the program, each student had to apply the knowledge he/she got to construct an autonomous vehicle and program it to achieve a number of tasks arranged in the form of a group competition. Eighteen secondary school students participated in the activities with the help of five IEEE Student members. The event was a great success and everyone enjoyed the experience.

IEEE Technical Community Spotlight
Fernando Guarin Educating Future Engineers

Reprinted from www.ieee.org/spotlight/

"As a child, I was always curious to learn how things worked," admits Fernando Guarin, 2016–2017 President-Elect for the IEEE Electron Devices Society (EDS). "I wondered, for instance, how it was possible to transmit voice or audio without wires. Later on, I watched my older brother build amplifiers and assemble HAM radios from kits when he was studying electrical engineering, so I followed in his footsteps." It is no small coincidence that this early exposure to building devices influenced a desire later in life to educate others. Guarin, recipient of the 2014 IEEE Meritorious Achievement Award in Informal Education, awarded for his dedication to bringing the excitement of electronics engineering to high school students, describes his method as "reaching young minds with 'hands-on' activities that are fun, build self-esteem, and enhance confidence in their own abilities."

Guarin earned his Bachelor's degree in electrical engineering from the Pontificia Universidad Javeriana in Bogotá, Columbia. Then, after graduation, he started working in Silicon Valley for National Semiconductor, and transferred with them to Tucson, Arizona, where he earned his MSEE from the University of Arizona. "After graduation, I joined IBM where I worked for 27 years; in 1993, I was selected by IBM for the Ph.D. resident work study program through a competitive program and was able to attend Columbia University where I earned my Ph.D. in electrical engineering." Guarin found that work experience very well complemented his academic studies, and in 2015, after retiring from IBM, joined Global Foundries where he is currently a Distinguished Member of Technical Staff working as the team leader for the 14 nm SOI technology qualification.

Guarin states enthusiastically, "I am living proof of the tremendous influence that IEEE can have on a professional career! I was a student member during my undergraduate studies. I rejoined as a professional member during my MSEE studies, and have been a member for 28 years." Guarin's extensive history within the organization is something of which he is tremendously proud. He started volunteering at the local level at the Mid-Hudson Section's EDS Chapter in New York's Hudson Valley and eventually became Chapter chair. He then became regional editor for the EDS newsletter and continues, today, to be active in the IEEE Mid-Hudson Section. Guarin has also been very involved in EDS, completing a term as Secretary, and now serving as 2016–2017 EDS President-Elect.

One of Guarin's proudest accomplishments with the organization, however, is the formation of the Engineers Demonstrating Science: an Engineer Teacher Connection (EDS-ETC) program, which grew out of outreach with local schools using simple snap circuits. "When former EDS President Renuka Jindal visited our Chapter in New York, he saw the potential to spread this outreach program to the whole world using our student and professional Chapters." The program has primarily relied on the snap circuits offered by Elenco™.

After conducting countless sessions with the program, Guarin reflects: "The strongest memories I have from the many sessions we have conducted are the children's smiles, their sense of accomplishment when they make their circuits work. Many have said, 'I thought I was not good at science, but now I have changed my mind.' The most gratifying moments are when, at the end of the session, the children want to continue 'playing'."

This is the perfect model to attract children to a future in engineering – especially since it is the one that garnished interest for Guarin, initially. Says Guarin, "I have come to the realization that, as engineers, we have a huge marketing problem. Many bright minds get turned off before they can reach their full potential. We have to dispel the "nerd" myth and show that science and engineering really are a lot of fun – and, as an aside, one can make a very decent living while contributing to make the world better." And it is extremely important to ensure a pipeline of future engineers. "The world needs more engineers and scientists to overcome the many problems we face today. Some of the most pressing problems are climate change, water shortages, pollution, and overcrowding of cities, to name a few."

In order to solve this challenge, Guarin suggests the value of similar outreach. "It is easy to criticize and point out problems," he says, "but the key question is, 'What can you do to solve them?'." Guarin's advice is, "Become engaged with your local community, try to train the teachers and other grownups. Every person that flips a light switch should be able to understand the basic concept of an electrical circuit."

Organizations like the IEEE can help, as well, by utilizing their global outreach. Says Guarin, "It is very powerful to have Chapters in every corner of the world. [The IEEE] has a wealth of trained engineers and practitioners that can easily transmit their knowledge. There is also the support structure and many initiatives like tryengineering.org and trynano.org, where they can access a wealth of materials, including lesson plans." But there are also opportunities for improvement: "There should be a concerted effort at IEEE to better communicate. Every Society has its own education committee, but these committees don't communicate across Societies. There should be a platform for doing so." And with so many dedicated volunteers, like Guarin, this is an attainable goal to better ensure the future of engineering and its introduction to the next generation.

Volunteering is a serious commitment, but the resulting joy and satisfaction are very rewarding. To find out more about the EDS-ETC outreach program, please visit http://eds.ieee.org/the-eds-etc-program.html.

EDS Webinar on Nanometer-Scale III–V CMOS

Presented by: Jesus A. del Alamo, Massachusetts Institute of Technology

EDS is many things to its members–scientific publisher, technical conference sponsor, networking resource–but at its core EDS is a community of learning. From undergraduate students and PhD candidates to tenured professors and world-renowned researchers, EDS provides device engineers from across the spectrum engaging and enriching educational opportunities.

As part of our commitment to enhancing the value of membership in EDS, we are pleased to present the EDS Webinar Archive. The online collection provides our members with on-demand access to streaming video of past events. The following recently held webinars can be found here, http://eds.ieee.org/webinar-archive.html.

Nanometer-Scale III–V CMOS

In the last few years, as Si electronics faces mounting difficulties to maintain its historical scaling path, transistors based on III–V compound semiconductors have emerged as a credible alternative. To get to this point, fundamental technical problems had to be solved though there are still many challenges that need to be addressed before the first non-Si CMOS technology becomes a reality. Among them, harnessing the outstanding electron transport properties of InGaAs, the leading n-channel material candidate, towards a high-performance nanoscale MOSFET has proven difficult; contact resistance, offstate characteristics, reliability and Si integration remain serious problems. Introducing a new material system is not the only challenge. Scalability to sub-10 nm gate dimensions also demands a new 3D transistor geometry. InGaAs FinFETs, Trigate MOSFETs and Nanowire MOSFETs have all been demonstrated but their performance is still disappointing. To compound the challenge, a high-performance nanoscale p-type transistor is also required. Among III–Vs, InGaSb is the most promising candidate. Planar MOSFETs have been demonstrated but more advanced geometries remain elusive. This talk will review recent progress as well as challenges confronting III–V electronics for future CMOS logic applications.

QuestEDS

Learn More About QuestEDS
QuestEDS is an important benefit of being an EDS member. Are you interested in knowing why it's not possible to measure the built-in voltage of a PN junction using a voltmeter? Do you need to understand the best way to derive an expression for the average thermal velocity of an electron? Or are you curious about what quantum dots and wires are? The answers to these questions and more are available through QuestEDS.

Below is a sample of what you can expect to find in the QuestEDS Library. **Want to see more, join EDS today!**

Question:
What are the major differences between the MOSFET models that are required for digital and analog circuit simulation/design using CMOS technology? What is the extent of additional MOSFET parametric characterization required for analog circuit design when compared to digital? Do the various CMOS fabrication houses generally characterize all the available technology libraries for both digital and analog applications?"

Answer:
Both analog and digital circuit simulation requires models which accurately describe the DC currents and terminal charges of the MOSFET as a function of the applied bias. MOSFETs in digital circuits sweep through a range of voltages during a switching event and the integrated current and total change in terminal charge must be accurate. In an analog circuit many devices experience small AC signals around a fixed DC bias point. For analog simulation, the derivatives of the current and charges with respect to the applied biases must also be accurate. For logic models, accurate off-state leakage currents are important for determining standby power which is typically less important in analog application. For either analog or digital models, the measurements of current and low frequency capacitance at many bias points are taken and used for modeling. In some cases smaller voltage steps are used to get more accurate derivatives for analog models.

In addition, if the analog circuit is operated at frequencies above 0.5 GHz accurate parasitic capacitances become important. These are normally measured using a network analyzer to measure S-Parameters. The term "RF model" is commonly used to describe a model which has been tuned to match such high frequency measurements.

The capabilities of CMOS models vary depending on the maturity of the technology and the intended application. Semiconductor foundries typically provide modeling reports which describe how the model was generated what usages it is intended for and provide some typical plots of the model overlaid on lab measurements.

New IEEE eNotice Express in vTools

vTools.eNotice is an email distribution service, provided by IEEE Member and Geographic Activities (MGA). This updated release, eNotice Express, has been developed to send newsletters, meeting notices, social events, and IEEE conference materials to members on behalf of volunteers.

Up until now, all eNotices required staff to process them, which could take up to 5 business days. eNotice Express removes the staff component and the wait time for delivery.

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The initial release of eNotice Express is available for Regions, Sections, Subsections, Councils, and Chapters.

vTools FAQS: http://sites.ieee.org/vtools/2016/01/11/enotice-faqs/

Chapter News

IEEE Spokane Celebrates 103 Years of Activity

By Steve Simmons

The IEEE Spokane Section celebrated its 103rd Anniversary this summer with a special celebration and party for Section members, guests from nearby Sections, IEEE friends and corporate and individual allies.

After 103 years of ups and downs, the Section was glad to celebrate that Spokane membership has increased in a dramatic and award-winning amount by this summer of 2016, as the economy in the Spokane metro area continues to diversify and expand in the ongoing aftermath of the Great Recession.

Attendees enjoying Spokane Section's 103rd Anniversary celebration

Appropriately, the event took place at a newly restored historic Spokane setting: Overbluff Cellars in the Historic Washington Cracker Building, 304 W. Pacific Ave, Spokane, Washington. The event was held on the evening of Thursday July 21, and featured great food and beverages, a gourmet BBQ dinner, and other festive enhancements! Special features included Spokane's own Overbluff Cellars wines, and other locally made hard cider and craft beers – as well as live music performed by a three piece local band playing everything from country to rock! Spouses and significant others were welcomed.

The Spokane Section enjoyed a great summer party and also, the kickoff for an expanded year of events to come. Coming events will include technical meetings focused on cyber security, robotics advances and regional developments in electric power.

Inaugural Event of the EDS/SSCS Hawaii Chapter

By John Borland

The IEEE Hawaii Section joint EDS/SSCS chapter, which was formed in February 2016, held their first event sponsoring two Distinguished Lecture Seminars on Friday, June 17th. This event took place after the VLSI Technology and Circuits Symposia, also held in Hawaii. Professor Jiann-Shiun Yuan, EDS Distinguished Lecturer, presented a lecture on the *"Internet of Things and Wearable Electronics: Ultra-Low Power and Hardware Security,"* where he discussed emerging research topics in this rapidly growing field. Professor Makoto Ikeda, SSCS Distinguished Lecturer, presented a lecture on the *"Basics of CMOS Image Sensors,"* where he discussed image sensor processes, noise characteristics of CMOS image sensors, and dynamic range extension techniques.

Professor Makoto Ikeda (left), SSCS Distinguished Lecturer and Professor Jiann-Shiun Yuan (right), EDS Distinguished Lecturer

EDS Distinguished Lecturers Mini-Colloquium GaN HEMT Technology, Modeling and Applications

By Daniel Tomaszewski

Extensive works in the field of GaN substrate and device fabrication have been conducted by several Polish companies and research groups. A Pol-HEMT project (http://www.polhemt.ite.waw.pl/en/home.html), coordinated by Instytut Technologii Elektronowej (ITE), Warsaw, was aimed at design and fabrication of a new type of microwave S-band HEMT transistor based on AlGaN/GaN structures, grown on bulk semi-insulating GaN substrates manufactured using an ammonothermal method. Within the project the AlGaN/GaN HEMT fabrication technology was proposed and test devices were manufactured (Fig. 1).

In order to establish a platform for exchange of expertise in the area of GaN technology, to share the Pol-HEMT achievements with an international community, and to attract interest from potential partners, the

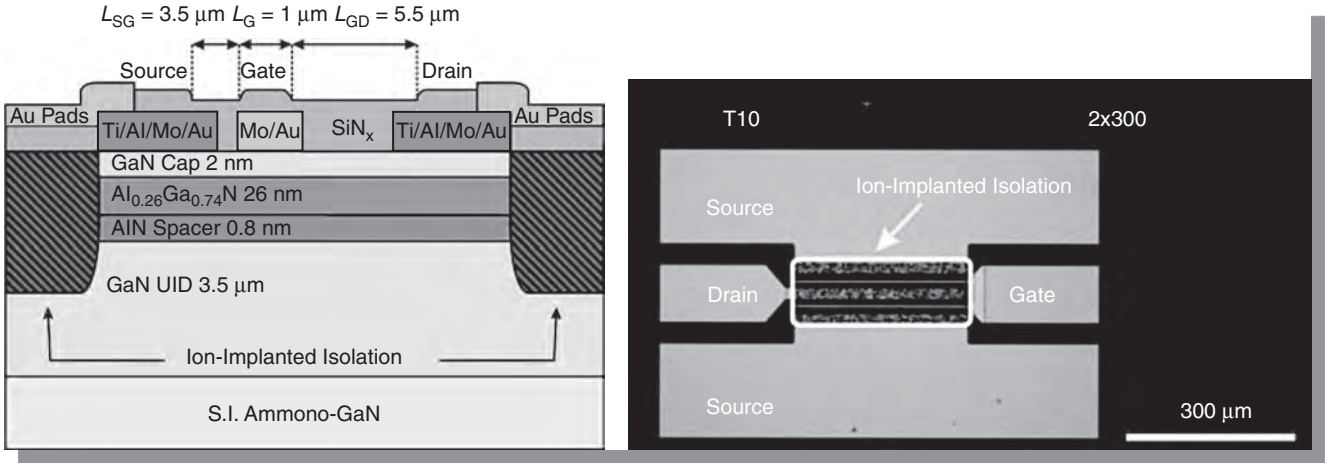


Fig. 1. Cross-section and optical microscopy image of 2-gate AlGaN/GaN HEMT fabricated under Pol-HEMT project after: A. Taube et al., Phys. Stat. Sol. A 212, No. 5, 1162–1169 (2015).

Participants of the Mini-Colloquium in Lodz, Poland

IEEE EDS Distinguished Lecturers Mini-Colloquium was organized by ITE, celebrating this year its 50th Anniversary. Technical support was provided by the Department of Microelectronics and Computer Science (DMCS), Lodz University of Technology and financial support provided by EDS. The Mini-Colloquium program covered the following domains: physics of wide bandgap semiconductor devices, technology of GaN HEMTs, tools and developments in the area of the HEMT modeling and selected aspects of the device applications including RF, power and THz detection domains. During the event eight talks were given:

1. M. S. Shur (DL), *"Physics of III-N-based Field Effect Transistors"*
2. M. Nawaz (DL), *"Current status of wide bandgap device research from power system perspective"*
3. P. Prystawko, *"MOCVD epitaxy on bulk GaN substrates for HEMT RF application"*
4. A. Taube, E. Kamińńska, A. Piotrowska, M. Ekielski, M. Myśśliwiec, W. Wojtasiak, M. Kozubal, J. Kaczmarski, A. Szerling, R. Kruszka, A. Trajnerowicz, M. Wzorek, M. Góralczyk, D. Kuchta, P. Prystawko, M. Zając, R. Kucharski, *"Development of AlGaN/GaN High Electron Mobility Transistors on Semi-Insulating Ammono-GaN Substrates"*
5. W. Knap, N. Dyakonova, D.But, F. Teppe, J.Suszek, A. M. Siemion, M. Sypek, G.Cywinski, K.Szkudlarek, I. Yahniuk, *"Terahertz Imaging With GaAs and GaN Plasma Field Effect Transistors Detectors Arrays"*
6. M. Zając, R. Kucharski, *"Highly resistive GaN substrates obtained by ammonothermal method for microwave applications"*
7. M. Brinson, V. Kuznetsov, D. Tomaszewski, *"Compact modeling of GaN HEMTs"*
8. W. Grabinski (DL), D. Tomaszewski, *"FOSS TCAD/EDA tools for compact modeling and its Verilog-A standardization"*

The Mini-Colloquium was attended by approximately 25 participants, including lecturers and audience. It was a successful event, triggering discussions during its duration and hopefully stimulating further joint projects.

EDS Mini Colloquium Held at Globalfoundries, USA – "New Frontiers in Electron Devices"

By Mukta Farooq

On August 11, 2016, an EDS Mini Colloquium jointly sponsored by the ED Mid-Hudson Valley Chapter and GlobalFoundries, was held at Malta, New York. In addition to EDS members from the Mid-Hudson Valley chapter, there were also 25 members from the local Schenectady EDS chapter, as well as from Rensselaer Polytechnic Institute (RPI) and Rochester Institute of Technology (RIT). The total audience for this session was 300.

The events included a plenary session with five speakers, including four EDS Distinguished Lecturers. The forum was well-received by all attendees and was an excellent opportunity for learning about new frontiers in electron devices.

Mini-Colloquium sponsored by the ED Mid-Hudson Valley Chapter and GlobalFoundries

The Plenary Session consisted of the following speakers.

Dr. Gary Patton, *IEEE Fellow and CTO & SVP, WW R&D, GlobalFoundries* – Opening Remarks

Dr. Fernando Guarin, *IEEE EDS DL, IEEE Fellow and GlobalFoundries DMTS* – "Si Devices – Evolution"

Dr. Mukta Farooq, *IEEE EDS DL, IEEE Fellow and GlobalFoundries Fellow* – "Paradigm Shifts in Packaging Technology"

Dr. Jamal Deen, *IEEE EDS DL, IEEE Fellow and Distinguished Professor, McMaster University* – "Smart

MQ Speakers: (left to right), Jamal Deen, Fernando Guarin, Mukta Farooq, Gary Patton, Rao Tummala, and Seung Kang

Sensors for Environmental and Health Applications"

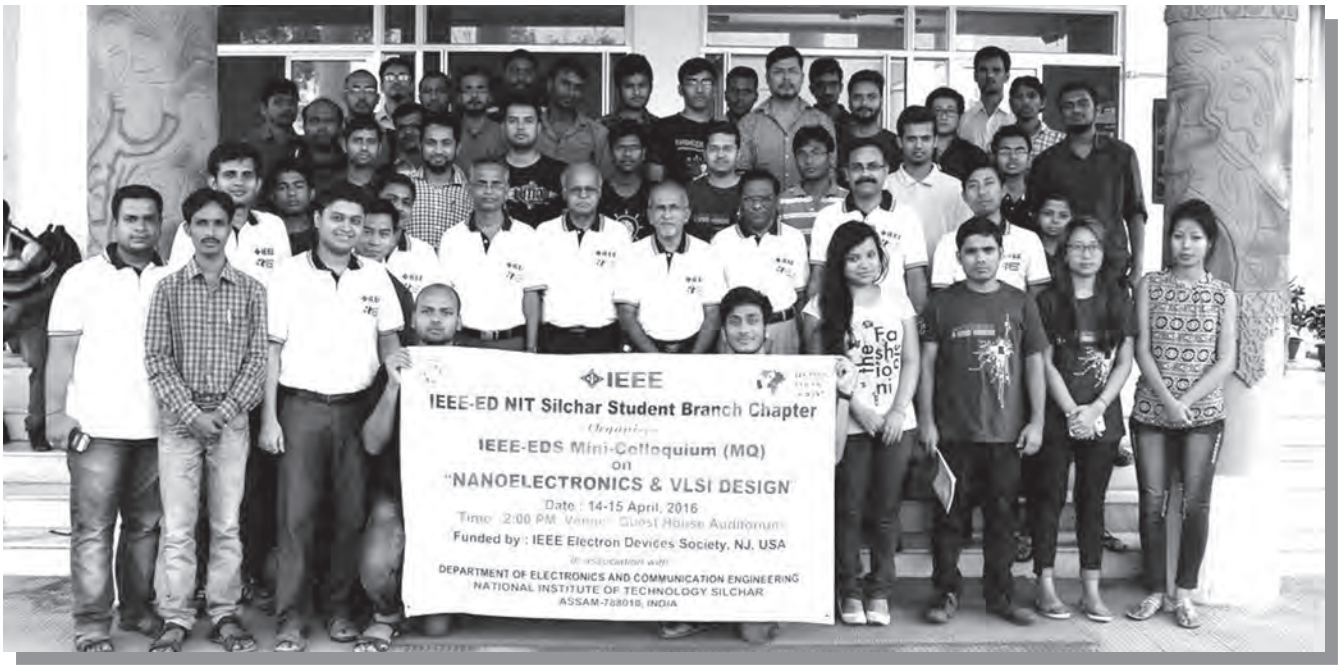
Dr. Seung Kang, *IEEE EDS DL and Director of Engineering, Qualcomm,* "Emerging Memory Architectures for IOT (Internet-of-Things) and Wearables"

Dr. Rao Tummala, *IEEE Fellow and Electronics Packaging Chair, Georgia Tech* – "System Scaling: The Other Electronics Frontier For A New Era of Consumer, Computer and Automotive Applications."

EDS Mini-Colloquium on "Nanoelectronics and VLSI Design"

By T R Lanka

The ED NIT Silchar Student Branch Chapter, India, organized its first ever Mini-Colloquium (MQ) on the theme "*Nanoelectronics and VLSI Design*" in association with the Department of Electronics and Communication Engineering, NIT Silchar, Assam, India, April 14–15, 2016. EDS Distinguished Lecturers, Dr. M. K. Radhakrishnan, Prof. S. K. Sarkar, Prof. G. N. Dash, and Prof. A. K. Panda delivered lectures on various subjects related to the theme of Mini-Colloquium. The most notable topics addressed during the MQ were interface mechanisms in MOS devices, geometries of MOSFETs and low power VLSI circuit designs, Quantum tunneling, and Graphene field effect transistors. Prof. A. K. Panda delivered a talk on Chip design with focus on IoTs and demonstrated his IMEC fabricated Chip. Dr. Radhakrishnan and Prof. G. N. Dash also enlightened the participants with the practice of research publishing in journals of repute. A total of 60 participants attended the two-day event.



Participants of the EDS MQ at NIT Silchar, (from left) Mr. Rupam Goswami (Student Chair: front position) Prof. F. A. Talukdar (Branch Counsellor, ED NIT Silchar SBC), Prof. S. K. Sarkar (EDS DL),Dr. M. K. Radhakrishnan (EDS DL), Prof. G. N. Dash (EDS DL), and Dr. T. R. Lenka (Faculty Advisor ED NIT Silchar SBC)

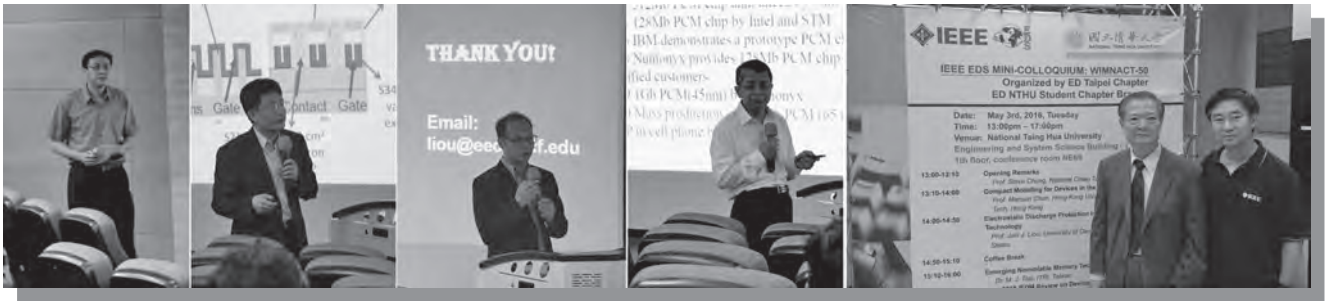
IEEE EDS Mini-Colloquium: WIMNACT-50 in Hsinchu, Taiwan

By Steve Chung And Chih-Fang Huang

The 50th IEEE EDS Mini-Colloquium on Nanometer CMOS Technology (WIMNACT-50) was held in Hsinchu, Taiwan, at National Tsing Hua University, on May 3, 2016. This workshop was sponsored by the Electron Devices Society and co-sponsored by the ED Taipei Chapter, ED NTHU Student Chapter Branch, and the organizing committee of ISNE 2016. It marks a milestone of the WIMNACT series since its inception in 2003.

This half-day workshop included lectures covering important perspectives of advanced CMOS technologies, compact modeling, electrostatic discharge protection, and non-volatile memory. Four professors and experts from the United States, Hong Kong, and Taiwan, including three EDS Distinguished Lecturers, were invited to deliver the outstanding talks. Over 120 registered students, professors, and research staff from academia as well as engineers and professionals from industry were in attendance.

Professor Steve Chung of National Chiao Tung University, Chair of the ED Taipei Chapter, commenced the workshop by welcoming all participants and giving them an overview of EDS activities, including the history of WIMNACT to encourage and promote membership. Then, Prof. Mansun Chan from Hong Kong University of Science and Technology, Hong Kong, gave his lecture entitled *"Compact Modeling for Devices in the Post-Moore Era,"* which addressed fundamental but important concepts in compact modeling of generic nano-scale transistors from circuit and industry point of views. He also introduced an interactive modeling and on-line simulation platform established through the efforts of his lab and other international universities and institutes. Immediately after, a lecture on *"Electrostatic Discharge Protection in 28-nm CMOS Technology"* was delivered by Professor Juin J. Liou, from the University of Central Florida in the United States. Functionalities and critical design issues for ESD device in circuitries for real applications



(From left) C. F. Huang (Workshop Chair), H. C. Lin(speaker), J. J. Liou (speaker), M. J. Tsai (speaker), Steve Chung (General Chair), Mansun Chan (speaker)

WIMNACT-50 participants, May 3, 2016: (1st row from left) Steve Chung (General Chair), C. F. Huang (Workshop Chair), M. J. Tsai (speaker), Mansun Chan (speaker), J. J. Liou (5th, speaker)

were touched upon. A few examples based on 28-nm platform were given and discussed. After a short break, Dr. Ming-Jinn Tsai, Research Director of the Electronic and Optoelectronic System Research Laboratories in ITRI, Taiwan, gave a lecture on *"Emerging Nonvolatile Memory Technology,"* in which the most recent advances and bottlenecks in cutting edge memory technologies such as Flash, MRAM, RRAM, and PCM, were overviewed with the pros and cons of each technology compared and discussed. The last lecture entitled of the event, *"Post-2015 IEDM Review on Device Technologies for 5 nm-node and Beyond,"* was given by Professor Horng-Chih Lin from National Chao-Tung University, Taiwan. He summarized the most important results and observations from last year's IEDM, and pointed out the trends in current CMOS technologies. Also, the challenges faced by some emerging device technologies such as III-V MOSFETs, Tunneling FETs, Negative-Capacitance FETs, and 2-D channel FETs were explained. During Q & A time and after the workshop, the speakers exchanged ideas and opinions intensely with the audience.

Overall, this event was very successful in bringing in local students and professionals, and bridging them with world-renowned experts through the distinguished lecturer program provided by EDS. After the workshop, all the attendees showed a strong interest in future distinguished lectures as well as other EDS activities. Some attendees and speakers stayed a few more days participating in the IEEE ISNE 2016 conference, which was scheduled for the next day in the same campus.

Steve Chung
General Chair of WIMNACT-50
Chih-Fang Huang
Workshop Chair of WIMNACT-50

A One-Day Workshop and a Student Paper Contest Held by ED Calcutta Chapters

By Atanu Kundu, Angsuman Sarkar, Swapnadip De, Manash Chanda And Swapnadip De

A One-Day workshop was held at Meghnad Saha Institute of Technology (MSIT) on April 20th. The event, with two invited EDS Distinguished Lecturers, was organized by the ED Meghnad Saha Institute of Technology Student Branch and the ED Meghnad Saha Institute of Technology Student Branch Chapter, in association with the IEEE Kolkata Section, ED Calcutta Chapter, HITK ED Student Branch Chapter and the Department of ECE, Meghnad Saha Institute of Technology.

The lectures, given by Professor Chandan Kumar Sarkar, Professor of ETCE Department of Jadavpur University and Professor Subir Kumar Sarkar, Professor of ETCE Department of Jadavpur University were attended by 60 participants, of whom 25 were IEEE members. All the participants benefited immensely from these talks.

Professor Subir Kr. Sarkar with the organizers and participants at the One-Day workshop at MSIT

The organizers and participants in the 1st IEEE MSIT Student Paper Contest 2016

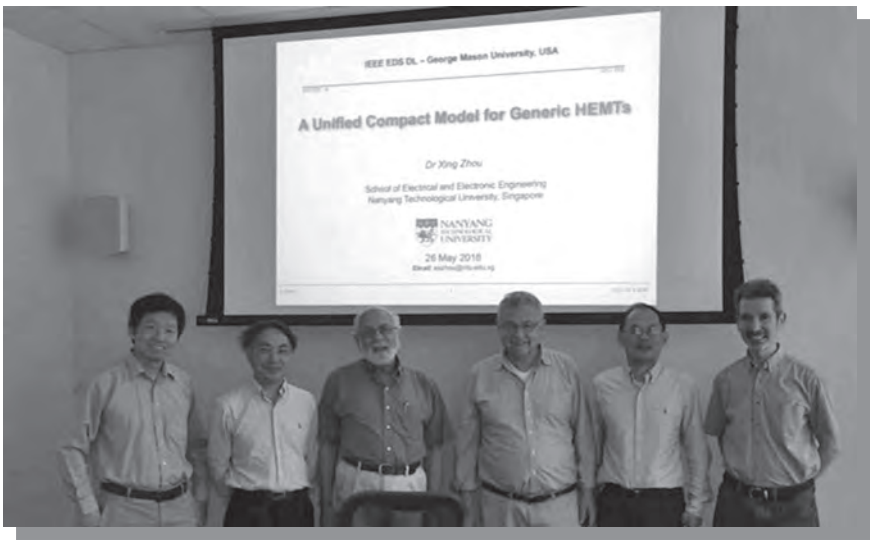
The "1st IEEE MSIT Student Paper Contest-2016" was organized by the IEEE MSIT Student Branch, in association with the ED MSIT Student Branch Chapter, the ED Calcutta Chapter and the Department of ECE, MSIT, on May 23rd. Seven selected groups presented their papers in front of eminent judges. The program was attended by 190 participants, of whom, 1 was an IEEE Senior Member and 30 IEEE members. On June 1st, the student branch chapter awarded certificates and mementos to the best three groups.

EDS Distinguished Lectures

IEEE EDS Distinguished Lecture Held at ED Northern Virginia/Washington DC Chapter

By Dimitris Ioannou

On May 26, 2016, we were pleased that EDS Distinguished Lecturer Dr. Xing Zhou, from the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, visited us here in Northern Virginia/Washington DC area and gave a very interesting lecture. This event was sponsored by the ED Northern Virginia/Washington DC Chapter and hosted by Professor Dimitris Ioannou, Department of Electrical and Computer Engineering, George Mason University. Dr. Zhou's lecture focused on the compact modeling of high electron-mobility transistors (HEMTs). He also highlighted his current research work and explained the future applications for III-V HEMTs devices.



(From left to right), Dr. Qiliang Li, Dr. Xing Zhou, Dr. Nadim Haddad, Dr. Dimitris Ioannou, Dr. John Zhang, and Dr. Martin Schulman

IEEE EDS Distinguished Lecture at Concordia University

By K. Karim

Prof. Karim S. Karim of the University of Waterloo was invited by the Electron Devices Society Montreal Chapter to deliver an EDS Distinguished Lecture, titled *"Ultra-high resolution amorphous selenium-CMOS hybrid X-ray imagers for bioengineering applications,"* at Concordia University, Montreal, Canada, on July 15, 2016.

The talk highlighted current areas in bioengineering and life sciences where ultra-high resolution X-ray imagers can find new application. X-ray imaging is a valuable alternative for *in vivo* imaging of small animals such as mice in genomics and cancer research. Active discussion was conducted after his talk.

Prof. Karim (left) presenting at Concordia University

IEEE EDS Distinguished Lectures Held in China

ED Beijing Chapter
—by Kangwei Zhang

On May 5, 2016, Prof. Hiroshi Iwai from Tokyo Institute of Technology visited the ED Beijing Chapter. With the Chapter's arrangement, he delivered an EDS Distinguished Lecture entitled, *"End of the scaling theory and the world after that."* The event was held at the Institute of Microelectronics of Chinese Academy of Sciences.

Prof. Iwai first introduced that the feature size of integrated circuits would reach its limits because of the structural limit, the electrical limit and the merit limit. What would happen after we reach the limit? Prof. Iwai explained that in a single integrated circuit chip level, Moore's law would end, but it was virtually extended through the internet connection. It would be an exciting period, and everyone would have a chance because most of the environment was already ready for use – nanofabrication processes and tools, nano device/process simulators, and knowledge of nano materials. The only necessary things needed are excellent ideas for application and successful business models. Long term, it would become important to use the existing bio systems as much as we could with the combination of semiconductor devices. The new points of his research made a big splash and reached an academic discussion.

On June 24, 2016, Prof. Ziqiang Qiu from UC Berkeley, gave an EDS Distinguished Lecture entitled, *"A*

Prof. Hiroshi Iwai (lecturer, first row, third from left), and Prof. Ming Liu (Beijing Chapter Chair, first row, second from left) with professors and student members

Professor Ziqiang Qiu was giving the EDS Distinguished Lecture

synthesis and study of artificial magnetic skyrmions" hosted by the ED Beijing Chapter at the Institute of Microelectronics of Chinese Academy of Sciences.

A magnetic skyrmion is a topological twist of two-dimensional spin texture which exhibits many fascinating properties. Prof. Qiu fabricated single crystalline Co disks on perpendicularly magnetized Ni/Cu (001) film to create artificial skyrmions whose topology could be tailored by changing the relative orientation between the vortex core polarity and the surrounding perpendicular magnetization. In this way, Prof. Qiu studied the topological effect of the skyrmion using Photoemission Electron Microscopy (PEEM). By applying an in-plane magnetic field of various strengths, Prof. Qiu found strong evidence that the annihilation of the vortex core depended on the topological skyrmion number of the system.

ED Guangzhou Chapter

—by Zhangang Zhang

The ED Guangzhou Chapter held an EDS Distinguished Lecture on May 24, 2016. Dr. Chai Yang from The Hong Kong Polytechnic University was invited to present a lecture entitled, *"Two-Dimensional Layered Materials for Future Nanoelectronics - Transistor and Interconnect."* In the DL, Dr. Chai Yang introduced the background motivations firstly, then the applications of two-dimensional layered materials (mainly graphene, MoS2, WSe2 and PtS2) in nanoelectronics as barrier and channel materials in detail. Researchers, engineers and students from China CEPREI Lab., South China University of Technology, Jinan University, et al., who attended this event enjoyed the discussions with Dr. Yang. Collaboration opportunities are anticipated between institutions in Southern China in the ED field.

ED Dalian Chapter

—by Zhengxing Huang

Professor Jiang Hu, IEEE Fellow, from Texas A&M University, gave an EDS Distinguished Lecture about optimization techniques for analog ICs on May 4, 2016. At first, Prof. Hu introduced optimization for real world problems with a short tutorial. The second part of this tutorial will demonstrate this process with a case of successful application in industry. Then, he introduced built-in self optimization for variation resilience of analog filters. At deep sub-micron integrated circuit technologies and beyond, characteristics of analog circuits are increasingly affected by process variations and device aging. In this talk, a built-in self-optimization technique was introduced. It enables that each analog IC chip can autonomously improve its performance in the presence of significant variations. As a demonstration, an on-chip analog self-test platform was implemented to test an active-RC band-pass filter, whose components can be reconfigured to obtain different frequency responses. The desired response is found by a digital circuit implementation of multi-start meta-heuristic optimization. The proposed technique does not rely on external test equipment or any general purpose digital signal processor. Its effectiveness is confirmed by simulations as well as measurement results from a test-chip fabricated in 180 nm CMOS technology.

Professor Jiang Hu during his lecture on May 4, 2016

ED Xi'an Chapter

—by Hongliang Lu

On June 3, Dr.-Ing. Oleg Cojocari, CEO of ACST GmbH, Germany, delivered an EDS Distinguished Lecture entitled *"Film-Diode Process Technology for Millimeter-and THz-Wave Application"* at Xidian University. This talk was hosted by the ED Xi'an Chapter. Dr. Cojocari mentioned film-diode process for THz electronics, Schottky-based component development in THz frequency band, quasi optical Schottky diode detectors for fast ultra-wideband detection, and some applications in European Space Agency (ESA) space programs, which greatly aroused the students' interest. After the talk, Dr. Cojocari answered several technical questions about the details in THz IC packaging and different methods to increase doubling efficiency. He also discussed with some attendees about possible developing trends of THz-technology, future technical problems, possible cooperating programs for key technical areas and plans for building a Sino-German cooperation platform.

Dr.-Ing. Oleg Cojocari giving the EDS Distinguished Lecture at Xidian University

On June 2nd, Prof. Jin Zou, a professor shared between the School of Mechanical and Mining Engineering (Materials Engineering) and the Centre for Microscopy and Microanalysis, at the University of Queensland, Australia, presented an EDS Distinguished Lecture at Xidian University, on the impact of catalysts in the growth of epitaxial III–V semiconductor nanowires. Prof. Zou introduced that III–V semiconductor and their hetero-structures had been paid extraordinary attention in recent years due to their unique structural and chemical characteristics and turn potential properties in optoelectronic, nanoelectronic, and sensing developments. Then, he explained that in general, semiconductor nanowires are induced by catalysts, which mediate the one-dimensional growth. Many nanowires induced by the catalysts have their own structural characteristics, since the complications of catalysts in inducing the nanowire growth. At last, Prof. Zou also summarized their discoveries of impact of catalysts in the growth of epitaxial III–V semiconductor nanowires for the past decade.

~ Ming Liu, Editor

ATTENTION!

Your Chapter Could Be Missing Important Notices and Funding Opportunities!

Please remember, whenever there is a change to Chapter Officers, both IEEE and EDS must be notified.

Please follow these two steps:

1. Report officer changes to IEEE via the vTools Officer Reporting form: https://officers.vtools.ieee.org/ (access to vTools requires use of an IEEE account).
2. Report officer changes to EDS by completing the Chapter Chair Update Form: https://ieeeforms.wufoo.com/forms/pgu6n1i1ixepnu/

Thank you in advance for your assistance.

16th International Workshop on Junction Technology (IWJT)

—by Yulong Jiang

The 16th International Workshop on Junction Technology (IWJT) was held by the ED/CPMT Shanghai Chapter on May 9–10, 2016, in Shanghai, China. During its 16 year history, the IWJT has always been an open forum focusing on the needs and interests of the community of junction formation technology in semiconductors. This year's conference was a big success with the concerted effort and thorough preparation of all the committee members. Twenty-two high-quality papers were submitted and 4 sections were held, displaying the main breakthroughs for doping, annealing, contact, characterization, simulation and materials technology. Prof. Hiroshi Iwai gave an overall view of the Moore's Law development and Prof. Yun Wang reported the challenges and new approaches of annealing technology from millisecond to nanosecond period. There were so many excellent reports in this meeting, which not only created a platform where over 60 participant experts can intercommunicate, but also contributed to the junction technology development with solutions to critical current issues.

7th International Nanoelectronics Conference (INEC 2016)

—by Haicheng Yao and Zhiwei Liu

The ED Chengdu Chapter organized the 7th International Nanoelectronics Conference (INEC 2016) at the Crowne Plaza Hotel, Chengdu, China, May 9–11, 2016. The conference was co-organized by the University of Electronic Science and Technology of China. This conference served as a forum for researchers from China and different parts of the world to share their research works in the field of nanoelectronics.

The INEC 2016 technical program consisted of 81 oral and 122 poster papers. In addition, the conference featured 3 keynote and 80 invited papers presented by top scientists or engineers. Some of the papers will be selected for publications in an edited book by Springer Publisher and 4 journal special issues in *Vacuum, IEEE Transactions on Nanotechnology, Microelectronics Reliability, and Solid State Electronics.*

The INEC 2016 opening ceremony was held on the first day, where it was hosted by Dr. Juin J. Liou, a professor at the University of Central Florida and a General Co-Chair of the conference.

Following the opening ceremony of the conference were three keynote speeches by renowned speakers:

- Prof. Chung-Yu Wu of National Chiao Tung University, Taiwan, delivered a talk entitled *"Implantable Medical Electronic Devices for Neuro-Modulation Processes for Future Nano- materials Processing;"*
- Prof. Seiji Samukawa of Tohoku University, Japan, delivered a talk entitled *"Atomic Layer Etching, Deposition and Surface Modification Processes for Future Nano-materials Processing,"* and
- Dr. Dong-Won Kim of Samsung Electronics Co., Korea, delivered a talk entitled *"Nano-electronic Devices Technology in Logic Applications."*

During the three-day event, about 300 researchers shared their latest research findings and ideas in oral and poster sessions in areas related to nano-materials, nano-photonics, nano-electronic devices and circuits, optoelectronics, modeling/simulation, MEMS/NEMS, nano-fabrication, energy devices, nanoscale memory and high speed device.

~ Ming Liu, Editor

Audience listening to one of the INEC keynote speeches, (right) Dr. Juin J. Liou presenting a plaque to Dr. Chung-Yu Wu, one of the INEC keynote speakers

28th ISPSD´2016, Prague, Czech Republic

By Jan Vobecky, High Voltage Subcommittee Chair

The 28th International Symposium on Power Semiconductor Devices & ICs (ISPSD´2016) was held from June 12–16, 2016, in Prague, Czech Republic. The mission of this event is to cultivate an international forum for professionals in the field of power semiconductor devices and smart power integrated circuits and related fields to meet regularly and exchange ideas and promote the growth and development of this field. Technical sponsorship of ISPSD has been provided by the IEEE Electron Devices Society (EDS) and co-sponsorship has been provided by European Center for Power Electronics (ECPE) and IEE Japan (IEEJ). The symposium attracted 479 registrants; 234 from Europe, 81 from Japan, 68 from North America and 96 from various other regions.

Visitors to the conference enjoyed the unique architecture of Prague on the way to the venue

The main program was preceded by short course lectures built around high-performance switches, starting with reviewing how wide bandgap semiconductors drive performance versus the ultimate optimization and limitations of mature silicon technology. Besides a lecture on packaging, there were two lectures on applications, namely power supplies and electrical vehicles. In the subsequent four days, the participants had opportunities to listen to four invited plenary talks, given by experts from industry and academia. Besides the investor´s view on the semiconductor industry (KKR), wide bandgap semiconductors for electric vehicles (Nissan), high-power devices for energy sector (GEIRI) and the role of GaN & SiC switches for high density power supplies (ETH) were also presented.

Furthermore, 40% of the 262 submitted papers and 23 of the late news were divided between Low Voltage, High Voltage, SiC, GaN, Integrated Power, and Packaging sessions. This gave the historically lowest acceptance ratio of 40%. For the first time, the wide bandgap devices were divided into two separate tracks, which resulted in three strong tracks: High Voltage, SiC and GaN. Because of the record high amount of submissions, two parallel oral sessions were introduced and the poster session was split into two days.

The Charitat Award for the Best Student Paper was presented to Hao Feng, for the paper entitled *"A 1200 V-Class Fin P-Body IGBT with Ultra-narrow-mesas for Low Conduction Loss."*

The Best Poster Award was presented to H. J. Schulze, for the paper entitled *"Use of 300 mm Magnetic Czochralski Wafers for the Fabrication of IGBTs."*

ISPSD´2017 will be held in Sapporo, Japan. See http://www.ispsd2017.com/.

23rd International Conference "Mixed Design of Integrated Circuits and Systems" (MIXDES 2016)

By Mariusz Orlikowski

On June 23–25, 2016, Łódź, Poland, the annual International Conference MIXDES 2016 took place. The event was organized by the Lodz University of Technology together with the Warsaw University of Technology. The conference was co-sponsored by the IEEE Poland Section ED and CAS Societies, Polish Academy of Sciences, Committee of Electronics and Telecommunication, Section of Microelectronics and Sections of Signals and Electronic Circuits and Systems and Commission of Electronics and Photonics of Polish National Committee of International Union of Radio Science – URSI.

The three-day program included 103 papers comprising of invited speeches, as well as oral and poster presentations, reviewed and selected from submissions from 21 countries.

In addition to the regular program, there were five invited speakers:

- *Advanced Amplification Techniques for Nanoscale CMOS Technologies* João P. Oliveira (Universidade Nova de Lisboa, Portugal)
- *Big Data and Electro-Thermal Design* Adam W. Skorek (University of Québec at Trois-Rivières, Canada)
- *CMOS FD-SOI Technology in the Eyes of a Circuit Designer* W. Kuźmicz (Warsaw University of Technology, Poland)
- *Nanoscale MOSFET Modeling for the Design of Low-power Analog and RF Circuits* Christian Enz (EPFL, Switzerland)
- *Terahertz Compact SPICE* Michael Shur (Rensselaer Polytechnic Institute, USA)

The sessions also included presentations in the frame of three special sessions:

- *Compact Modeling for RF Circuit Design* organized by Dr. Daniel Tomaszewski (Institute of Electron Technology, Poland) and Dr. Władysław Grabiński (GMC Suisse, Switzerland)
- *Data Acquisition and Control Systems in Industry and High Energy Physics* organized by Dr. Stefan Simrock (ITER, France) and Dr. Dariusz Makowski (Lodz University of Technology, Poland)
- *Nanoscale Thermal Modelling and Measurement* organized by Dr. Marcin Janicki (Lodz University of Technology, Poland)

Some of the attendees at the 2016 MIXDES Conference

The authors of selected papers received Best Paper Award diplomas and the ED Chapter in the IEEE Poland Section presented the Young Scientist Paper Award to Patricia Carla Petrut, for the paper entitled "Configurable FPGA Architecture for Hardware-Software Merge Sorting."

MIXDES 2017 will take place in Bydgoszcz. The Preliminary Call for Papers is available at http://www.mixdes.org/downloads/call2017.pdf. More information about past and upcoming MIXDES conferences can be found at http://www.mixdes.org.

23rd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)

By Dave Tan

The 23rd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA) 2016 was held at the vibrant Marina Bay Sands Exposition and Convention Centre, Singapore from July 18 – 21, 2016. IPFA 2016 is organized by the ED/CPMT/Reliability Singapore Chapter. The Symposium is technically co-sponsored by the IEEE Electron Devices Society and the IEEE Reliability Society. This year is special for the IPFA as we are celebrating its 30th Anniversary. In conjunction with the anniversary celebrations, a brand new IPFA logo has been launched.

IPFA is devoted to the fundamental understanding of the physical mechanisms of semiconductor device failures and issues related to semiconductor device reliability, yield and performance; especially those related to advanced process technologies. For IPFA 2016, more than 100 abstracts were submitted in the vastly improved and revised 6 technical tracks. There were 4 technical tracks on Failure Analysis and 2 technical tracks on Reliability. The abstracts were subjected to a thorough technical review by an international panel of experts.

IPFA 2016 featured a keynote speech by leading industry expert,

Dr. John Y. Xie, who is Director of Packaging Technology Research and Development at Altera/Intel Corp on the topic of "More than 2D: The Industry Wide Challenge." Another keynote speaker is leading researcher Prof. KL Pey, who is the Associate Provost of the Singapore University of Technology and Design on the topic of "Design for Reliability of nano-devices and systems." A video preview of the keynote talks is available on the newly launched IPFA YouTube channel.

A one-day tutorial involving 6 short courses was held on Day 1 of the conference. Besides covering courses on the fundamentals of FA and Reliability, there were also courses on more advanced topics like GaN Reliability, Fault Isolation through Advanced Optics, 3D Interconnect Reliability and Nanoscale Debug. The Symposium had 13 invited talks on a wide range of topics related to failure analysis and reliability. The tutorial and invited talks were given by leading researchers from top universities/research institutions and industry experts from all over the world.

The evening workshop was a new program introduced this year. In the workshop, participants had an opportunity to discuss challenges in physical failure analysis such as FIB sample preparation, defect imaging, device deprocessing, nanoprobing and materials characterization. The workshop aimed to provide an excellent forum for engineers, researchers and tool developers to informally meet and exchange experiences, viewpoints and resolve challenges that they are facing.

Another hallmark of the IPFA was the Equipment Exhibition by leading vendors, with a record number of 36 exhibitors who showcased their technologies and state-of-the art tools. A session was also included in the Symposium for the exhibitors to present/highlight their tools & equipment innovations. The challenges faced by FA and Reliability practitioners often need the latest tools and techniques to resolve and the newly-introduced session greatly addressed those needs.

IEEE Workshop on Microelectronics and Electron Devices Organized by ED Boise Chapter

By Jaydeb Goswami

More than 400 attendees, including students, university professors, and semiconductor engineering professionals gathered at Boise State University on April 15, 2016, for the 2016 IEEE Workshop on Microelectronics and Electron Devices (WMED). This workshop provided a forum for discussion on different aspects of silicon and non-silicon technologies and inspired students and professionals in the Treasure Valley to exchange their ideas with world renowned researchers. In its 14th year, the workshop brought several distinguished speakers to discuss a variety of trending topics, including wearable technologies, 3D device architectures, and emerging memory technologies.

Invited speakers and members of organizing committee at 2016 IEEE WMED

For the last nine years, the WMED has successfully arranged a high school program in parallel with the main conference in order to support the effort of encouraging STEM education among students in the Treasure Valley area. This year's high school program was a half day event which included a keynote talk by Jim Nottingham, Vice President of the LaserJet and Enterprise Solutions Hardware Portfolio at Hewlett Packard, and a panel discussion of engineers from all age groups who related their experiences and took questions from the students about careers in engineering. The students also participated in hands-on activities organized by Dean Klein, Micron Technology's Vice President of Memory System Development, and Laurie Anderson, Micron's K-12 Education Manager.

Dear EDS Chapters:

When planning your upcoming chapter meetings, workshops, etc., please remember to visit the EDS website for a recent list of EDS Distinguished Lecturers and lecture topics.

Checklist

- Chapter contacts EDS DL to check availability, confirms date/location of lecture, discusses DL funding needs and determines chapter funding
- EDS DL completes EDS DL Activity Log and Funding Request Form
- If applicable, obtain EDS funding approval
- Chapter publicizes lecture via web, email, etc. Obtain a chapter member list via SAMIEEE (http://www.ieee.org/about/volunteers/samieee/index)
- If applicable, DL submits an IEEE expense report to Laura Riello, to receive reimbursement
- Chapter Chair/DL Coordinator submits an EDS DL/MQ Feedback Form

If you have any questions and/or need more information, please do not hesitate to contact Laura Riello, EDS Executive Office.

Thank you for your continued support of the Society.

IEEE Journal of the Electron Devices Society

The IEEE Journal of the Electron Devices Society (J-EDS) is a peer-reviewed, open-access, fully electronic scientific journal publishing papers ranging from applied to fundamental research that are scientifically rigorous and relevant to electron devices.

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- Worldwide audience;
- Increased dissemination;
- High impact factor (IF),
- Articles can be cited sooner;
- Articles potentially cited more frequently.

Regional News

Europe, Middle East & Africa (Region 8)

ED/MTT/CPMT/SSC/COM Central Ukraine Chapter

—by Yuriy Yakimenko, Volodymyr Timofeyev, Yuriy Poplavko

In the period of April 19–21, 2016, the 36th International Scientific Conference "Electronics and Nanotechnology" (www.elnano.kpi.ua) was held at National Technical University of Ukraine "Kiev Polytechnic Institute."

The ELNANO conference inherits the annual conferences in electronics, founded in 1980 by Professor Vitaliy Sigorski, a well-known scientist in the field of electronic circuit theory. A main organizer is the Faculty of Electronics (departments of Physical and Biomedical Electronics, Microelectronics and Nanoelectronics, and Industrial Electronics). Among the conference organizers is also the National Aviation University of Ukraine and the Institute of Semiconductor Physics of Ukrainian Academy of Sciences. Since the 2013 ELNANO, the conference has been supported by the IEEE Ukrainian Section (Central Ukraine Joint Chapter, IEEE Kiev Student Branch and others).

The conference was attended by over 150 participants. Apart from the Ukrainian scientists, the conference gathered researchers and young scientists from Armenia, Belarus, Canada, Estonia, France, Georgia, Germany, Great Britain, Italy, Spain, Lithuania, Mexico, Montenegro, Netherlands, Poland, Turkey and USA. The working language of the conference and of the proceedings was English.

Two plenary sessions and three workshops: *"Micro- and nanoelectronics," "Biomedical Electronics and Signal Processing," and "Electronic Systems"* were held. The first workshop was organized on the initiative of Prof. Martin Kirchner (Dortmund, Germany). The other two workshops were organized by the Department of Design of Electronic Computing Equipment (Head – Prof. O.M. Lysenko) and were focused on problems of telecommunication and systems on a chip (SOCs). A special session of the X-ray and tomography systems was chaired by Prof. S. Miroshnichenko, who represented a NPO "Teleoptic" company involved in medical technology and information and algorithmic support system diagnostics. NPO "Teleoptic" was one of the sponsors of the conference.

During the conference, reports were presented on the following topics: modern nanotechnology and its application in biomedical electronic, micro- and nano-electronics components, methods of electronic circuit and system design, signal and image processing, prospects for biomedical device and system development. Scientific works were selected for presentation by more than 80 experts from 15 countries (at least three reviewers for each report). This meets the requirements of conferences organized under the auspices of the IEEE and entitles it to include the Proceedings in the IEEE *Xplore* Digital Library, which is indexed to Scopus, Google Scholar and others data bases.

There were also fruitful debates on opportunities for international cooperation and implementation of joint research projects involving a wide range of national and international scientific organizations.

~ Daniel Tomaszewski, Editor

Asia & Pacific (Region 10)

ED Kansai Chapter

—by Michinori Nishihara

The ED Kansai Chapter held the 14th International Meeting for Future of Electron Devices, Kansai (2016 IMFEDK) at Ryukoku University Kyoto Hall, Kyoto, Japan, June 23-24, 2016, with the theme of "What are the next key devices for IoT era?"

The meeting attracted 108 attendees and was preceded by a tutorial seminar with two Distinguished Lecturers:

1) "The Coming SiC/GaNAge - Emerging Package and Analysis Technologies" by Dr. Satoshi Tanimoto of Nissan Arc, and
2) "Oxide thin-film transistor technology and its application to flexible displays" by Dr. Mitsuru Nakata of NHK Science & Technology Research Laboratories.

The formal program began after the tutorial session with opening remarks by the general chair Prof. Yasuhisa Omura. The two day program featured a keynote titled *"Quest for Visual System of the Brain to Create Artificial Vision"* by Prof. Tetsuya Yagi of Osaka University. There also were five invited papers: 1) *"Detection and Characterization of Single MOS Interface Traps by the Charge Pumping Method"* by Prof. Toshiaki Tsuchiya of Shimane University; 2) *"Heterogeneous integration of SiGe/Ge and III-V on Si for CMOS photonics"* by Prof. Mitsuru Takenaka of The University of Tokyo; 3) *"High Quality Free-standing GaN Substrates and Their Application to High Breakdown Voltage GaN p-n Diodes"* by Prof. Tomoyoshi Mishima of Hosei University; 4) "*High Resolution Silicon MEMS Tactile Sensors for Measurement of Fingertip Sensation"* by Prof. Hidekuni Takao of University of Kagawa; 5) *"Transverse Thermoelectric Effect and Its Applications using Synthetically or Naturally Anisotropic Materials"* by Dr. Tsutomu Kanno of Panasonic Corporation. In addition there were 11 papers in three regular technical sessions and a poster session of 28 posters with

2016 IMFEDK Awards Winners and Poster Session

topics covering Silicon, Compound, and Emerging Technologies. There were many student discussions in front of their posters during the poster session.

At the end of the meeting the following awards were presented:

- IEEE EDS Kansai Chapter IMFEDK Best Paper Award, to Yuichiro Nanen of ROHM Co., Ltd.
- IEEE EDS Kansai Chapter IMFEDK Student Paper Award, to the following four persons: Masataka Shirasawa (Osaka University), Taisei Yamazaki (University of Fukui), Le Thi Yen (Osaka University), Itaru Raifuku (NAIST).

The award winners were congratulated warmly by all participants. IMFEDK will continue to encourage and contribute to our student members in the Kansai area by providing opportunities to present their ideas in English, hence extending their technical network to other countries.

~ Kuniyuki Kakushima, Editor

ED Taipei Chapter

—by Steve Chung

The ED Taipei Chapter together with the EDS NCTU Student Chapter held two invited talks in the third quarter of 2016, with the first on July 15th given by Distinguished Lecturer Prof. J. H. He, (King Abdullah University of Science and Technology), Chair of the ED Western Saudi Arabia Chapter. Prof. He's lecture entitled, *"Flexible, Foldable and Multi-Functional Paper-Based Electronics,"* began with a review of current studies on paper electronics for flexible applications. Paper, as a flexible, foldable, cost-efficient and mass productive substrate, has shown diverse applications for flexible electronics. First, he presented the first nonvolatile resistive memory using paper as substrates by means of all-printing techniques. Then, he introduced the algorithm of Origami art into the device design for flexible electronics, such as photodetectors and nanogenerators, taking advantage of the foldability and adaptability of paper substrates. In particular, paper origami triboelectric nanogenerators using paper as the starting material, with high degree of flexibility, light weight, low cost, and recyclability was presented. This talk was attended by around 50 graduate students, professors, and post-doc researchers.

The second talk given by Prof. Peide Ye, from Purdue University, USA, was entitled, *"New Channel Materials and Devices Beyond Si CMOS."* Prof. Ye first reviewed state-of-the-art technology development in recent years on III–V and Ge MOS technology by industrial and academic leaders. He also presented some new progress at Purdue University related to important results that have been developed, including the first GaAs and Ge CMOS circuits demonstration. At or even beyond 5 nm node, the device channel must be atomic layer thin to

ED Taipei Invited Talks on July 15th (seated left) Prof. H. C. Kuo, Prof. Steve Chung, and Prof. J. H. He (speaker, from KAUST); and July 28th Prof. Peide Ye (speaker, from Purdue)

Prof. Gaskov (left), Prof. Rumyntseva (right)

avoid the short channel effects. The emerging 2D materials could be one of the solutions. He then presented two 2D semiconducting materials – MoS2 as n-type channel and phosphorene as p-type channel with more recent results. In addition, the unique material property of the newly pioneered phosphorene and its potential for various device applications was demonstrated. This talk was attended by around 40 graduate students, professors, and post-doc researchers.

One major upcoming event is the regional conference IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC 2017), with EDS as a co-sponsor and key members of the local chapter involved. The conference venue is at Tsing Hua University, Hsinchu, Taiwan, and scheduled to begin on October 18th. Please make a note on your calendar for paper submissions in mid-2017.

~ Ming Liu, Editor

ED/MTT/SSC Penang-Malaysia Chapter

—by Wong Peng Wen

The IEEE Penang Chapter held a technical talk on April 29, 2016. The talk, titled *"IoT and Low Voltage Analog Design for Wireless Applications"* was presented by Professor S. S. Jamuar of the University of Malaysia Perlis. The talk presented an overview of the Internet of Things (IoT) and the importance of low voltage low power design technique. Prof. Jamuar gave attendees a brief overview of current trends in the development of low voltage design techniques for analog circuits in wireless applications. He also presented different analog design techniques and how these techniques are expected to find use in analog circuits used in IoT components.

A dual-technical talk was held June 6, 2016. The first talk, titled "'IoT

Prof. Jamuar giving a technical talk on IoT

Technical talks by Prof. Jeoti and Prof. Chakrabarti at UTP

of Passive Things and SAW RFID System" was presented by Prof. Varun Jeoti of the University Teknologi Petronas. The talk revisited Surface Acoustic Wave (SAW) based RFID, which is an RFID that is passive and can be read from a distance wirelessly. He also presented on the premise that they can become part of this IOT revolution. The second talk, titled "*Real-Time Task Scheduling on FPGAs*" was presented by Prof. Amlan Chakrabarti, from the University of Calcutta, India. The talk briefed on the preliminary concepts of embedded processing on FPGAs using hardware cores and also some of the scheduling strategies in regards to efficient mapping of hardware tasks on reconfigurable cores. All the talks were well attended by people from both industry and academia.

IEEE and EDS Members along with Interim Executive Members of IEEE EDS Uttar Pradesh (U.P.) Section-Kanpur Chapter

IEEE Senior Membership Elevation Workshop

The IEEE Penang Joint Chapter hosted a IEEE Senior Membership Elevation Workshop at Penang Skills Development Center (PSDC) on May 28, 2016. The speaker was Dr. Mohammad Faizal bin Ahmad Fauzi, vice chair of the IEEE Malaysia Section. The workshop was attended by 11 IEEE members from both academia and industry. During the workshop, Dr. Faizal presented an overview of member grade elevation procedures, recognition and benefits of the senior member grade, requirements for senior membership elevation and case studies. After the presentation by Dr. Faizal, participants proceeded to the online application and had a chance to clarify with Dr. Faizal about their application while filling in the details in the particularly significant performance section. It was a fruitful workshop and the chapter hopes that participants will succeed in their applications.

Participants of the IEEE Senior Member Elevation Workshop

ED/CPMT/Reliability Singapore Chapter

—by Dave Tan

The chapter organized two technical talks; the first entitled "*Some Issues of MOS Gate Dielectric Scaling in Sub-nanometer EOT Range*" by Prof. Hei Wong from Zhejiang University, China / City University of Hong Kong on March 11, 2016 at SUTD. The second technical talk entitled "*VLSI for Space Applications, A New Paradigm*" was given by Dr. Philippe Perdu from CNES, France, on June 29, 2016 at NTU.

~ P Susthitha Menon, Editor

ED Uttar Pradesh Section – Kanpur Chapter

—by Yogesh Chauhan

The chapters' first meeting, inauguration ceremony and election of Executive Committee Members, was attended by more than 50 IEEE and EDS members from different institutions and universities. The meeting was conducted April 3, 2016, at IIT Kanpur, India. The meeting began with an introductory lecture on the benefits of IEEE and EDS membership for professional, technical and personal development. The informative lecture was delivered by the Chair of the Executive Committee of the chapter, Dr. Yogesh Singh Chauhan, Department of Electrical Engineering, IIT Kanpur, India.

Several attendees also gave their views on IEEE and EDS chapter activities and formation of the Executive Committee. The presenters were: Prof. S. Sundar Kumar Iyer, Department of Electrical Engineering, IIT Kanpur, Dr. Anshu Gaur, Department of Materials Science and Engineering, IIT Kanpur, Dr. Brijesh Kumar, Department of ECE, Madan Mohan Malaviya University of Technology, Gorakhpur (UP) and Dr. Rekha Verma and Dr. Sitangshu

Cake Cutting Ceremony at Inauguration of ED Uttar Pradesh Section-Kanpur Chapter

Bhattacharya, both from Department of ECE, IIIT Allahabad.

The chapter organized a Distinguished Lecture by Dr. Wladek Grabinski on *"Free and Open Source Software TCAD/EDA Tools for Semiconductor Device Modeling"* on April 11, 2016 at Indian Institute of Technology (IIT) Kanpur. New technology and device development were illustrated by application examples of FOSS TCAD tools like Cogenda TCAD and DEVSIM. Compact modeling was highlighted through topics related to parameter extraction and standardization of the experimental and measurement data exchange formats. Finally, two FOSS CAD simulation and design tools: ngspice and Qucs, were presented by the speaker. This Distinguished Lecture (DL) was attended by more than 40 participants and was very useful to all the researchers and engineers actively involved in the development of compact/SPICE models and design of integrated circuits, in particular at the transistors level.

ED KGEC Student Chapter, Kalyani

—by Angsuman Sarkar

The chapter, in association with the Department of ECE, Kalyani Government Engineering College and the ED Kolkata Chapter, organized the 1st International Conference on "Devices for Integrated Circuits (DevIC 2016)," March, 29–30, 2016, at Kalyani Government Engineering College. The proceedings of the conference included 32 papers that cover a wide spectrum of technological issues related to Devices for application in Integrated Circuits. Plenary talks were delivered by Dr. Writam Banerjee, Institute of Microelectronics of Chinese Academy of Science, Beijing, China, on *"Resistive Switching: an Emerging Technology"* and by Dr. Chandan Kr. Sarkar, Jadavpur University, Kolkata, India, on *"Impact of High K layer material on Analog/RF Performance of forward and reversed Graded channel Gate Stack DG- MOSFETs."* The talks were interactive with lively participation by the attendees. The conference was very well received by the more than 75 students and 50 faculty members who attended.

ED University of Calcutta Student Branch Chapter

—by Soumya Pandit

The Chapter organized a technical talk on *"IEEE Seminar on Art and Challenges of Writing Paper for IEEE Journals."* The lecture was held on April 29, 2016, at the Meghnad Saha Auditorium, Rajabazar Science College Campus, University of Calcutta. The speaker, Prof. Debatosh Guha, Professor, Institute of Radio Physics and Electronics, presented a comprehensive picture of the state of the art methods for writing papers for IEEE Journals. The talk began with the challenges faced by students while writing papers for IEEE Journals, which was followed by best methods and practices for writing various sections and sub-sections of the paper and concluded with the reviewer's point of view while approving a paper. Approximately 100 research scholars and students, as well as 25 faculty members attended the lecture.

Participants along with Prof. D. Guha at M. N. Saha Auditorium, University of Calcutta

ED VIT Chapter

—by Sivasankaran K

The ED VIT Chapter organized a five-day faculty development program on "*Analog Electronic Circuits*," May 31 to June, 4, 2016, by Dr. Roy P Paily, Professor, IIT Guwahati. The FDP started with an introductory note by Dr. K. Sivasankaran, Chapter Chair, who also gave an overview on IEEE EDS and its membership benefits.

ED VIT Chapter Five Day Faculty Development Program on "Analog Electronic Circuits"

ED Nepal Chapter, Kathmandu

—by Bhadra Pokharel

The chapter arranged a two day Training Program on Computational Physics,organized by Central Department of Physics, TU, Kirtipur, with the financial support of UGC, Nepal, May, 14–15, 2016. Day one's program was mainly concentrated on the basics of learning computational physics and programming from lectures, with the second day focused on practical or hands-on sessions. There were 6 lectures on May 14th and two hands-on- sessions on May 15th. The program was technically supported by ICTP, Italy. There was a total of 38 participants for this program from different institutions of TU, including IEEE members, Faculty of Physics and students.

Prof. Dr. Narayan Adhikari of CDP delivered a talk on Computational Physics: Applications to solve Physics problems with a few examples" and Dr. Elisa Fratini from ICTP delivered a talk on Solving Quantum mechanical problems using computation physics. In the post lunch session, Dr. Gopi Chandra Kafle and Mr. Nupati Pantha delivered talks on "Programming with Fortran I & II."

The ED Nepal Chapter and Kathmandu University, organized the one day National Symposium on '***Nanotechnology for Novel Materials Processing'*** on June 1, 2016, in Kathmandu University, Dhulikhel, Kavre. The program was technically supported by Chemical Science and Engineering and Natural School of Engineering, Kathmandu University and financially supported by University Grant Commission, Nepal.

Resource persons Dr. Elisa Fratini and Prof. Narayan Adhikari

Scenes from the 2016 NSNMP

There were 2 Keynote speakers, 2 invited lectures, 10 oral and 6 poster presentations, with 65 delegates who took part in the symposium. In the first session, Prof. Andreecz Huzko, Warsaw University, Poland, delivered his keynote speech on *"Graphene: Synthesis, properties and Applications."* The second talk was delivered by ED Nepal Chapter Chair, Prof. Bhadra Pokharel on *"Nano-Powder synthesis of Antiferroelectric* ($Pb_{1-x}Ba_x$) ZrO_3 *(*$0 \leq x \leq 0.15$*) Ceramics for Energy storage Devices."* Prof. Jerzy Jurewich of Universite de Sherbrooke, Quebec, Canada, delivered his keynote speech on *"Applications of nano-Powders in Electronics-case: The Multilayer Layered Capacitor Chip (MLCC)"* and Prof. Deepak Subedi, Associate Dean of KU, delivered his talk on *"Non-thermal Plasmas and their applications for Material processing."*

ED Delhi Chapter

—by Manoj Saxena

The Chapter organized an IEEE Distinguished Lecture on *"Silicon Nanodevices: Interface Physics and Analysis Challenges"* by Dr. M. K. Radhakrishnan, Vice President of Regions and Chapters, IEEE Electron Devices Society, on April 5, 2016, at Deen Dayal Upadhyaya College.

Dr. Radhakrishan gave another EDS DL, *"Engineering Evolution in Electronics and 50 years of Moore,"* on the same day at Indira Gandhi Delhi Technical University for Women, which was attended by more than 80 students and faculty members. The talk aimed at discussing the evolution of electronics to the modern day devices employing nano-technology in view of Moore's Law.

The chapter also organized for EDS members, an educational visit to Central Scientific Instruments Organization (CSIO) and Semi-Conductor Laboratory (SCL), Chandigarh, April 8, 2016. CSIO is a constituent unit of Council of Scientific & Industrial Research (CSIR), India, and is a premier national laboratory dedicated

Dr. Radhakrishnan, EDS Distinguished Lecturer, at Indira Gandhi Delhi Technical University for Women

to research, design and development of scientific and industrial instruments. The visiting group got the opportunity to get first-hand knowledge about different techniques involved in Optical fiber based nanoantenna fabrication, and its applications in optical tweezing, Optical fiber based chemical and biosensors and indigenous technology development for Head up Display for LCA.

The next leg of the trip to Semi-Conductor Laboratory (formerly known as Semiconductor Complex Limited, established in 1983), had the main objective to undertake, aid, promote, guide and co-ordinate Research & Development in the field of semiconductor technology, Micro Electro Mechanical Systems and process technologies relating to semiconductor processing. SCL, through its in-house R&D efforts, has developed 3 micron, 2 micron, 1.2 micron and 0.8 micron CMOS technologies, as well as specialized technologies such as EEPROM and CCD. The laboratory visit aimed to learn about the process steps required to develop a CMOS for 0.8 μm technology node. During the visit, a clean room tour was undertaken by all the members to understand the different processing steps, such as wafer etching (dry and wet etching), Implantation, Diffusion, Metallization, Defect detection and also packaging. The workings of various high-end instruments used for fabrication at both the front and back end, was explained.

Clean Room visit at Semi-Conductor Laboratory (SCL)

The chapter and Shaheed Rajguru College of Applied Sciences for Women, Vasundhara Enclave, Delhi, jointly organized the One Week short course on PLC and SCADA from May 25–31, 2016, which was attended by 6 delegates. The resource people for the short course were from Futuronix Automation Pvt. Ltd. The students learned about basics of PLC and SCADA, ladder logic using NO/NC switches, hardware connection of PLC and software knowledge on programming to work with these automation tools. They were also imparted hands-on training on PLC wiring kits and programming.

~ Manoj Saxena, Editor

EDS MEETINGS CALENDAR

The complete EDS Calendar can be found at our web site: http://eds.ieee.org. Please visit.

2016 11th European Microwave Integrated Circuits Conference (EuMIC)	3 - 5 Oct 2016	ExCeL London One Western Gateway Royal Victoria Dock London, United Kingdom
2016 IEEE International Integrated Reliability Workshop (IIRW)	9 - 13 Oct 2016	Stanford Sierra Conference Center 130 Fallen Leaf Road South Lake Tahoe, CA, USA
2016 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	10 - 13 Oct 2016	Hyatt Regency San Francisco Airport 1333 Bayshore Highway Burlingame, CA, USA
2016 International Semiconductor Conference (CAS)	10 - 12 Oct 2016	Rina Sinaia Hotel 8, Carol I str Sinaia, Romania
2016 16th Non-Volatile Memory Technology Symposium (NVMTS)	17 - 19 Oct 2016	Carnegie Mellon University 5000 Forbes Ave Pittsburgh, PA, USA
2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)	23 - 26 Oct 2016	Doubletree by Hilton Austin 6505 N IH 35 Austin, TX, USA
2016 7th International Conference on Computer Aided Design for Thin-Film Transistor Technologies (CAD-TFT)	26 - 28 Oct 2016	Beijing, China
2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)	7 - 9 Nov 2016	Hilton Garden Inn 1325 North Palak Drive Fayetteville, AR, USA
2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	7 - 10 Nov 2016	Doubletree by Hilton Hotel Austin 6505 N. Interstate 35 Austin, TX, USA
2016 11th International Conference on Advanced Semiconductor Devices & Microsystems (ASDAM)	13 - 16 Nov 2016	Smolenice Castle Zámocká Smolenice, Slovakia

2016 IEEE International Electron Devices Meeting (IEDM)	3 - 7 Dec 2016	Hilton San Francisco Union Square 333 O'Farrell St. San Francisco, CA, USA
2016 IEEE 47th Semiconductor Interface Specialists Conference (SISC)	7 - 10 Dec 2016	Catamaran Resort Hotel 3999 Mission Blvd. San Diego, CA, USA
2016 International Symposium on Semiconductor Manufacturing (ISSM)	12 - 13 Dec 2016	KFC Hall 1-6-1 Yokoami Sumida-ku Tokyo, Japan
2016 3rd International Conference on Emerging Electronics (ICEE)	27 - 30 Dec 2016	Indian Institute of Technology Bombay Powai Mumbai, India
2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM)	28 February - 2 March 2017	Toyama International Conference Center Toyama, Japan
2017 International Conference of Microelectronic Test Structures (ICMTS) Final submission deadline: 20 Jan 2017 Notification of acceptance date: 20 Nov 2016	27 - 30 Mar 2017	Minatec 3 Parvis Louis Néel Grenoble, France
2017 IEEE International Reliability Physics Symposium (IRPS) Final submission deadline: 01 Feb 2017 Notification of acceptance date: 21 Dec 2016	2 - 6 Apr 2017	Hyatt Regency Monterey One Old Golf Course Road Monterey, CA, USA
2017 IEEE International Memory Workshop (IMW) Abstract submission deadline: 08 Feb 2017 Final submission deadline: 11 Mar 2017 Notification of acceptance date: 01 Mar 2017	14 - 17 May 2017	Hyatt Regency Monterey One Old Golf Course Road Monterey, CA, USA
2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)	28 May - 1 Jun 2017	Royton Sapporo Kita 1 jyou nishi 11-1, Chuo-ku Sapporo, Japan
2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)	4 - 6 June 2017	Hawaii Convention Center Honolulu, Hawaii

2017 IEEE 44th Photovoltaic Specialists Conference (PVSC)	25 - 30 Jun 2017	Marriott Washington Wardman Park 2660 Woodley Road NW Washington, DC, USA
2017 International Siberian Conference on Control and Communications (SIBCON) Abstract submission deadline: 28 Feb 2017 Full Paper Submission deadline: 28 Feb 2017 Final submission deadline: 28 Apr 2017 Notification of acceptance date: 28 Mar 2017	29 - 30 Jun 2017	Sultanbek S. Isenov KATU Pobedy Ave., 62 Astana, Kazakhstan
2017 IEEE 44th Photovoltaic Specialists Conference (PVSC)	25 - 30 Jun 2017	Marriott Washington Wardman Park 2660 Woodley Road NW Washington, DC, USA
2017 International Siberian Conference on Control and Communications (SIBCON) Abstract submission deadline: 28 Feb 2017 Full Paper Submission deadline: 28 Feb 2017 Final submission deadline: 28 Apr 2017 Notification of acceptance date: 28 Mar 2017	29 - 30 Jun 2017	Sultanbek S. Isenov KATU Pobedy Ave., 62 Astana, Kazakhstan
2017 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) Abstract submission deadline: 21 Apr 2017 Final submission deadline: 21 Jul 2017 Notification of acceptance date: 14 Jul 2017	22 - 25 Oct 2017	Miami Marriott Biscayne Bay 1633 N. Bayshore Drive Miami, FL, USA
2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	12 - 16 Nov 2017	Irvine Marriott 18000 Von Karman Ave. Irvine, CA, USA
2017 IEEE International Electron Devices Meeting (IEDM) Abstract submission deadline: 01 Jun 2017 Final submission deadline: 01 Sep 2017 Notification of acceptance date: 01 Aug 2017	4 - 6 Dec 2017	Hilton San Francisco Union Square San Francisco, CA, USA
2018 IEEE International Reliability Physics Symposium (IRPS) Abstract submission deadline: 10 Oct 2017 Full Paper Submission deadline: 01 Jan 2018 Final submission deadline: 10 Jan 2018 Notification of acceptance date: 15 Dec 2017	11 - 15 Mar 2018	Hyatt Regency San Francisco Airport 1333 Bayshore Highway Burlingame, CA, USA

2018 IEEE International Vacuum Electronics Conference (IVEC) Abstract submission deadline: 22 Dec 2017 Full Paper Submission deadline: 22 Dec 2017 Final submission deadline: 02 Mar 2018 Notification of acceptance date: 02 Feb 2018	24 - 26 Apr 2018	Monterey Marriott 350 Called Principal Monterey, CA, USA
2018 IEEE 30th International Symposium on Power Semiconductor Devices and IC's (ISPSD) Abstract submission deadline: 31 Oct 2017 Full Paper Submission deadline: 31 Mar 2018 Final submission deadline: 31 Mar 2018 Notification of acceptance date: 31 Dec 2017	13 - 17 May 2018	Palmer House Hilton 17 East Monroe Street Chicago, IL, USA
2018 IEEE Symposium on VLSI Technology	12 - 14 Jun 2018	Hilton Hawaiian Village Honolulu, HI, USA
2018 IEEE International Electron Devices Meeting (IEDM)	29 Nov - 07 Dec 2018	Hilton San Francisco San Francisco, CA, USA

ELECTRON DEVICES SOCIETY®

EDS Vision and Mission Statements

Vision Statement

Promoting excellence in the field of electron devices for the benefit of humanity

Mission Statement

To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

Field of Interest

The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

The society is concerned with research, development, design and manufacture related to the materials, processing, technology, and applications of such devices, and scientific, technical, educational and other activities that contribute to the advancement of this field.

62nd International Electron Devices Meeting

DON'T MISS THESE SPECIAL EVENTS!

Prof. Roberto Cingolani
Istituto Italiano di Tecnologia

IEDM Luncheon

The IEDM luncheon will be held on Tuesday, December 6TH, 12:20 p.m. – 2:00 p.m.

This year's distinguished speaker is Prof. Robert Cingolani from the Istituto Italiano di Tecnologia, Genoa, Italy, who will give a presentation titled "Translating evolution into technology: from biochemical robots to autonomous anthropomorphic machines."

Vamsee Pamula
Co-founder of Baebies, Inc.

Entrepreneurs Luncheon

The IEDM Entrepreneurs Luncheon will be held on Wednesday, December 7TH, 12:30 pm – 1:30 pm.

Jointly sponsored by IEDM and IEEE Women in Engineering, the Entrepreneurs Lunch will feature Vamsee Pamula, co-founder of Baebies, Inc. a company developing digital microfluidics technology for newborn screening and pediatric testing. Pamula co-founded Baebies in 2014, following the sale of a predecessor microfluidics company that he also co-founded – Advanced Liquid Logic – to Illumina, Inc.

Vamsee has years of experience with digital microfluidics. He has served as Principal Investigator on several National Institutes of Health-funded projects, and has led many talks and published more than 60 articles, five book chapters and a book on the topic. He has more than 200 issued and pending patents, a PhD in Electrical and Computer Engineering from Duke University, and also serves as Adjunct Professor there.

The Inaugural **Electron Devices Technology and Manufacturing** (EDTM) conference is a full three-day conference to be held at Toyama International Conference Center, Japan, from February 28th to March 2nd, 2017, fully sponsored by the IEEE Electron Devices Society (EDS). EDTM is intended to serve as a forum for the electron devices community to collaborate on topics ranging from devices, materials, and tools, to create new and innovative technologies.

EDTM is structured to provide forums for Technical Sessions, Education (Tutorials, Poster Sessions and Short Courses) and Exhibition. Research papers on Electron Device Technology and Manufacturing related topics are solicited till November 4, 2016.

For more information, please visit the conference website, http://ewh.ieee.org/conf/edtm/2017

Ravi Todi, IEEE EDS VP for Technical Committees and Meetings

Shu Ikeda, EDTM Conference General Chair