IEEE
ELECTRON DEVICES SOCIETY
Newsletter

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Technical Briefs

Highlights of the 2017 IEEE Photovoltaic Specialists Conference

The international 2017 IEEE Photovoltaic Specialists Conference, also called PVSC-44, was held June 25–30, 2017, at the Marriott Wardman Park Hotel in Washington, D.C. The PVSC-44 is the leading international conference on PV science and technology and one of the flagship conferences of IEEE sponsored by the Electron Devices Society. Being a highly interactive venue for both seasoned PV experts as well as entry-level professionals and students, the PVSC-44 provided a unique opportunity to meet share and discuss PV-related developments in a timely, influential forum. The conference had therefore 1,298 attendees from 43 different countries out of which 57% came from the USA, 8% from Japan, 4% from Germany, 3% from Australia, 3% from China and the remaining 25% from other nations. During the conference, 986 presentations took place; 62% of these presentations were posters, which were partly shown by interactive e-poster boards.

The PVSC conference is well known for its strong awards program's. This year's recipient of the William R. Cherry Award was Eli Yablonovitch (Berkeley University, USA) in recognition of his many contributions to solar cell device physics and technology, among which strained semiconductor lasers and photonic crystals. The Young Professional Awardee was Weiwei Deng (State Key Laboratory of PV Science and Technology, China) for her work on the development of low cost mono- and multi-crystalline silicon PERC solar

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Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at edsnewsletter@ieee.org

ELECTRON DEVICES SOCIETY

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Newsletter Deadlines

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at http://eds.ieee.org/eds-newsletters.html. The archive contains issues from July 1994 to the present.

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Highlights of the 2017 IEEE Photovoltaic Specialists Conference

(continued from page 1)

cells with world record efficiencies. Richard King (Arizona State University, USA) was elevated to the level of IEEE Fellow. Further, many Best Student Paper Awards and Poster Awards were issued in various categories. A full listing of the award winners can be found on the PVSC-44 website under the Awards menu.

The PVSC-44's Technical Program included 12 areas covering cutting-edge developments in photovoltaics, ranging from fundamentals to applications, with an emphasis on material science, devices, PV systems, solar resources and policy. The PVSC-44 was opened by an excellent Keynote presentation by Charlie Gay (Department of Energy, USA). At present the technical program can be easily digitally explored at http://www.ieee-pvsc.org/PVSC44. However, to give the reader focused insights on the conference's vast program, this Technical Brief provides an overview of the conference highlights per area.

Area 1 was on *Fundamentals and New Concepts for Future Technologies* and kicked off with a Plenary talk by Jean-Francois Guillemoles of the IRDEP at CNRS, who spoke about hot carrier solar cells and some of the illusions surrounding them. After first presenting an excellent overview of hot carrier effects in semiconductors, he then described the hyperspectral photoluminescence imaging technique that allows the carrier temperature and electrochemical potential of electrons and holes to be determined unambiguously. Insights on hot carrier solar cell design included not simply requiring slowed cooling, but control of all of the processes, as well as the selective energy contact operation. Lars Samuelson of Lund University opened an exciting Nanowire (NW) Photovoltaics special session. Lars first reviewed the growth and applications of nanowire arrays in the early days, followed by the development of nanowire photovoltaics in nanophotonics. Topics include 15.3% record efficiency of GaAs NW in 2015, substrate reuse via NW thin film peel-off, and tandem junction NW cells. He also introduced the aerotaxy method of single crystalline NW synthesis as a low-cost means to the mass production of NWPV. Until recently, Selenium photovoltaics remained overlooked and stalled with a low efficiency record of 5%. Douglas Bishop from IBM T.J. Watson Research Center demonstrated a 30% increase in efficiency and a simultaneous reduction in thickness by a factor of five. Due to their bandgap, these low cost Se devices look very promising for indoor applications, such as powering Internet of Things (IoT) devices.

The Area 2, *Chalcogenide Thin Film Solar Cells*, Plenary was given by Dr. Markus Gloeckler from First Solar who spoke about the company's relentless advances in quality and efficiency and their record of moving drastic innovations in the cell technology into production within 2 years. First Solar is scaling production on 440 W_{peak} Series 6 modules that are over three times as large as prior modules. The use of CdSeTe bandgap grading to ~1.4 eV at the front of the cell increases J_{sc} dramatically, while ZnTe back

Winners of the Best Student Paper Award, (Back Left to Right) Geoff Bradshaw (Awards Chair), Ilke Celik, Klemens K. Ilse, Seonyong Park, Jeremie Werner, Bradley M. West, Mallory A. Jensen, Amit Munsh, Natasha E. Hjerrild, (From Left to Right) Angele Reinders (General Chair) and Seth Hubbard (Program Chair), (Student Award Winners not in photo) Sven Killinger, Xiaochen Zhang, Illya Nayshevsky, Boju Gai

contacting controls Cu migration thus making the modules extremely stable. As well, Area 2 had multiple presentations from First Solar, IEC Delaware, and NREL reporting significant advances in p-doping CdTe using P, As, and Sb rather than Cu, providing a strategy for reaching greater than 1 V V_{oc}. Walajabad Sampath's group at Colorado State University reported the highest-ever efficiency CdTe cell (not produced by First Solar) at 19.1%. Paul Haney of NIST detailed a recently developed analytical framework for V_{oc} loss from grain boundaries in polycrystalline solar cells including complex grain boundary networks. Lars Stolt of Solibro reported 17% modules and plans to double the module area to 1.88 m.

The Area 3 sessions on *III-V and Concentrator Technologies* were jam-packed this year, with lots of new and exciting work regarding III-V technology. Plenary speaker Stefan Myrskog, VP of Control Systems at Morgan Solar, provided an overview of their development of solid, thin-plate CPV modules using innovative optics concepts borrowed from the optical communications field. Their newest designs are based on a standard Si industry bill of materials and have applications ranging from cost effective utility scale generation to multi-purpose building integrated systems. Area 3 invited speaker Stephen Forrest (University of Michigan) discussed methods for wafer reuse requiring no polishing, as well as new tracker concepts based on kirigami, the Japanese art of paper folding and cutting. John Geisz of NREL gave an insightful tour of NREL's effort toward the development of a 6-junction concentrator cell. A special session was held this year dedicated to results from the ARPA-E MOSAIC program, with an introduction from invited speaker, and MOSAIC program manager, Michael Haney. A range of innovative and fascinating module designs were presented, with the goal of a Moore's Law type system level scaling for CPV. Finally, a joint session on "Hybrid Tandems" pitted III-V and perovskite based Si tandems in a battle for the best. Record results include a 32.3% 2-terminal III-V/Si cell (Frank Dimroth, Fraunhofer ISE), a 23.6% monolithic Perovskite/Silicon (Zhengshan Yu, ASU, in collaboration with Stanford) and 32.5% and 32.8% III-V/Si cells (Stephanie Essig, EPFL, in collaboration with NREL and CSEM). The two Most Outstanding Technical Contributions to the PVSC-44 were awarded in this area to Stephanie Essig for her III-V/Si dual-junction solar cells (Fig. 1a) and their challenging path towards cost competiveness, and Zhengshan Ju, who presented record results on monolithic perovskite/silicon tandem devices (Fig. 1b).

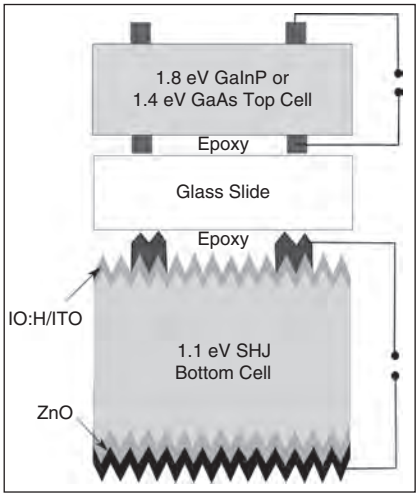

Fig. 1(a). Schematic cross section of the mechanically stacked III-V/Si dual-junction solar cells with record one-sun efficiencies up to 32.8% (© 2017 IEEE) Proceedings of the 2017 PVSC-44. "Mechanically stacked 4-terminal III-V/Si tandem solar cells" Stephanie Essig, Christophe Allebé, John F. Geisz, Myles A. Steiner, Loris Barraud, Antoine Descoeudres, J. Scott Ward, Manuel Schnabel, David L. Young, Matthieu Despeisse, Christophe Ballif, Adele Tamboli

Area 4 was on *Silicon Photovoltaic Materials and* Devices. The Plenary was given by Pietro Altermatt of Trina Solar. Pietro presented their most recent research in High-Performance (HP) multicrystalline p-type Si, showing that the reduction in dislocations due to the HP mc-Si process and the reduction in Fe impurities in the Si material has already allowed for a record efficiency of 21.25% (total area on 156 mm wafers). He also give a plan to reach efficiencies greater than 22% in the future. If contaminants such as Fe and Cu are sufficiently reduced, the performance of mc-Si can be as good as mono-crystalline CZ solar cells. In other Area 4 news, Kunta Yoshikawa (Kaneka) announced the current world record single-junction Si device using a backside contact hetero-junction structure with a 26.7% efficiency. Stefan Glunz (Fraunhofer ISE) reported on the development of TOPcon passivated contact cells with efficiency up to 25.3% and a world record n-type multi-Si cell with an efficiency of 21.9%. Weiwei Deng (Trina Solar) presented her research leading to a 22.61% efficient PERC Silicon solar cell. Johnson Wong (SERIS) presented on Griddler AI (artificial intelligence), a Luminescence Image Analysis program using a Finite Element simulator that seeks

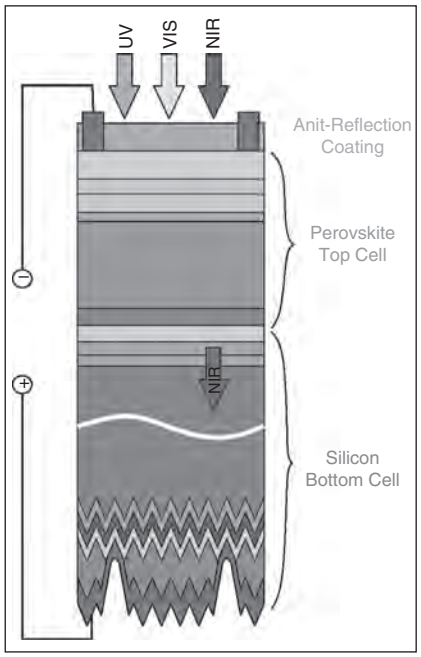

Fig. 1(b). Schematic of the monolithic Perovskite/Silicon tandem solar cell, with record-breaking efficiency of 23.6%

cell parameters that can best explain a set of luminescence imaging data. The fitted cell parameters (contact resistance spatial distribution, saturation current densities of the wafer's passivated regions and under the metal contacts) lead to simulated I-V characteristics that are in agreement with experimental data.

Area 5, *Characterization Methods,* had plenary speaker David Ginger from the University of Washington. He presented on the realization of correlative scanning and optical microscopies to probe perovskites. Informative photoluminescence maps of grains and interfaces before and after chemical treatment were also presented, showing a guideline to diagnose the sources of non-radiative recombination within any PV material. Area 5 also provided a fantastic special session on synchrotron-based characterization methods to advance the understanding of light-induced effects in perovskites. Laura Schelhas, from SLAC, discussed how in-operando X-ray diffraction reveals the relevant structural changes that take place in perovskites as a function of temperature. Jeremy Poindexter, from MIT, resolved the chemical composition distribution in perovskite grains with high spatial resolution by X-ray fluorescence. Finally, during a session on novel scanning probe microscopy approaches, Pablo Garrillo, from CEA in Grenoble, presented the use of multi-temporal photo-carrier dynamics at the nanoscale. As well, Julia Deitz, from Ohio State University, gave an outstanding presentation on how EELS can be realized to help us understanding the origin of deep level defects in CIGS.

In Area 6 *Perovskite and Organic Solar Cells*, Michael McGehee of Stanford University delivered an excellent overview on recent progress and development of perovskite solar cells. He showed promising thermal cycling results for addressing the big challenges to perovskites with stability results indicating the potential for long-term performance. The focus of his group's work is on improving stability and lowering costs and their work on a perovskite-silicon tandem devices was highlighted. As result of this work, a world record efficiency of 23.6% for 1 square centimeter monolithic perovskite Si tandem solar cell was demonstrated. Alex Zunger (University of Colorado) gave an exciting invited talk to discuss rational materials discovery for perovskites and the limitations and promise of newly discovered families of materials. Finally, both CSEM and EPFL demonstrated perovskite modules with steady-state aperture area efficiencies as high as 16% and a geometrical fill factor of 92.

For the Area 7 *Space and Specialty Technologies* plenary, we were pleased to welcome a talk from Christophe Allaud of OneWeb who presented on "Low Cost Applied to Large Constellations" for their ambitious goal to provide global high-speed internet access. Christophe's presentation demonstrated the manufacturing and automated assembly plans needed to achieve their production plans of over 900 satellites per year. The first generation of satellites plan to utilize triple junction III-V solar cells generating around 500 watts and would have an expected mission life of 6 years. Don Walker from Aerospace Corporation demonstrated that individual subcell parameters of a GaInP/GaInAs/Ge triple junction solar cell irradiated by 1 MeV electrons can be derived utilizing the spectral reciprocity relation between electroluminescence and external quantum efficiency. Gordon Wu and Bao Hoang from Space Systems Loral (SSL) discussed a new analytical tool for accurate shadow prediction of space solar, using a combination of CAD modeling, raytracing and simulation of solar cell performance under various levels of illumination. Louise Hirst from the Naval Research Laboratory presented results for ultra-thin GaAs cells with potential for superior radiation hardness.

In the Area 8 *PV Modules, Manufacturing, Systems and Applications,* Plenary Christophe Ballif of EPFL presented us with a fascinating overview of concepts for improving module performance as well as his concepts for unique PV applications. His work on PV modules that reflect light in the visible range drew the most attention. This interesting technology can be used to make white-looking modules but also unlimited textures and even images, thus hiding the fact that PV modules are present at all, and opening up additional applications where aesthetics trump economics. Kyumin Lee of CFV Solar Test Laboratory demonstrated that once the temperature dependence of the series resistance is included, the single-diode model can reproduce I-V curves with greater accuracy. Multiple groups presented on irradiance modeling for bifacial PV applications, showing significant progress and consistent results, including validations of field measured data. Bruce King of Sandia presented on the degradation of 6 CIGS modules typologies and observed two populations with respect to degradation in maximum power. One population of older products displayed a high degradation rate of 2%/year or greater while the second, contemporary population displayed degradation of less than 0.5%/year.

In the Area 9 *PV and System Reliability,* Plenary John Trout from Dupont summarized the use of field data and accelerated testing data to better understand materials durability. Data from 200 systems including 2 million modules showed 7.5% observation of problems with back sheets and 11% observation of problems related to cells. The accelerated test sequence correlating best with field data included damp heat, UV, and thermal cycling and found 1000 h of damp heat exposure correlated to backsheets and 2000 h correlated to cell corrosion. Dirk Jordan of NREL presented how year-on-year calculations of degradation rates are "the best thing since sliced bread." Olga Lavrova from Sandia

showed how several factors limit the potential shock hazard to firefighters encountering rooftop PV arrays, among them the resistances in their protective gear and the high effective resistance of ungrounded arrays. Nick Bosco (NREL) quantified the adhesion strength needed to avoid delamination in fielded modules. Robert Witteck (ISFH, Germany) presented UV light degradation of front surface recombination by breaking the H bond in SiNx. Finally, Volker Naumann of Fraunhofer CSP identified specific surface defects causing potential-induced degradation (PID).

The Area 10 *Power Electronics and Grid Integration* Plenary saw Thomas Bialek (San Diego Gas and Electric) first describe the current challenges of high penetration PV integration, including the variability issues of PV generation and the lack of high-temporal resolution visibility that utilities have traditionally used to operate their systems. Tom discussed how advanced PV inverter capabilities can mitigate many undesirable impacts by managing reactive power in the grid and buildings in bulk system support in distribution-connected PV to maintain overall system reliability. Mahesh Morjaria (First Solar Inc.) gave a well-received invited talk on reducing costs of installed solar energy, flexibility and Automated Generator Control (AGC) capabilities of PV. Sigfredo Gonzalez (Sandia) presented definitions and simulation results of 6 classes of PV inverter unintentional islanding capability.

In the Area 11 *Solar Resources for PV and Forecasting* Plenary, Steven Steffel of Pepco Holdings Inc. give a broad overview of some of the challenges faced when integrating renewables into the electricity grid and some of the opportunities for PV in particular to play a vital role on the grid of the future. He showed how the grid of the future will need advanced monitoring and secure communications for existing infrastructure, advanced modelling for geolocating generators, as well as smart algorithms in order to balance load and distributed generation. The importance of PV in terms of ancillary services such as voltage regulation will also continue to grow in the future. In a joint session with Area 10, Nicholas Engerer (The Australian National University) demonstrated a forecast of PV production in Australia, using the advanced Himawari satellite data (10 min., 1 km resolution), showing impressive accuracy for short term forecasts. Yu Xie (NREL), gave an excellent overview of a new improved rapid radiative transfer model for estimating solar resources from satellite observations. The Fast All-sky Radiation Model for Solar applications (FARMS) uses the simulation of clear-sky transmittance and reflectance and a parameterization of cloud transmittance and reflectance to rapidly compute broadband irradiances on horizontal surfaces. The accuracy of FARMS is comparable to that of two-stream approximation, but it is almost 1,000 times faster.

Finally, the Plenary talk for Area 12 *PV Deployment and Sustainability* featured Becca Jones-Albertus from the U.S. Department of Energy's SunShot Office. SunShot has set an aggressive cost target of 3 ¢/kWh by 2030 for utility-scale PV. Reaching this cost target would enable a tremendous future for PV, where photovoltaics could provide 15–20% of US electricity in 2030 and 30–60% in 2050. Area 12 also featured excellent regional updates from speakers from Japan, South Korea, Europe and the US. Strong growth is expected in most markets, with South Korea's government actively supporting PV, with an aim for 35 GW of installed capacity by 2030. Finally, in an invited talk by Vasilis Fthenakis (Columbia University), opportunities for clean water desalination and the role of photovoltaics were discussed. Reverse osmosis (RO) plants provide 75% of new desalination capacity, which requires constant power input. Vasilis discussed solutions in which PV, despite the intermittent nature, can provide a clean power source for RO.

In addition, several special international sessions took place on such topics as Smart Mobility, Grid Integration and TPV. There were many other activities such as 10 tutorials on key PV topics, an exhibit, several receptions, a high school program, a Young Professionals networking event, a PV jobs fair, a Women in PV Luncheon, a wonderful conference banquet in the National Air and Space Museum, a lovely social program, an "Open Mike Night" and the traditional early morning scheduled Sun Run. Next year the PVSC will be held at the Hilton Waikoloa Village in Hawaii in the form of a world conference, named WCPEC-7. The dates of this forthcoming event will be June 10–15, 2018.

The authors greatly acknowledge Jeremiah McNatt (NASA, USA), the full Program Committee and in particular PVSC-44's presenters for their contributions to the daily highlights and the realization of the technical program of the PVSC-44 conference. It was a great meeting for which we like to thank all involved!

This article was prepared by Dr. Stephen Bremner, the PVSC-44 Daily Highlights Coordinator, Dr. Seth Hubbard, the PVSC-44 Technical Program Chair, and Dr. Angèle Reinders, the PVSC-44 Conference Chair.

Upcoming Technical Meetings

2017 IEEE International Electron Devices Meeting

Advances in semiconductor and related devices are driving significant progress in our increasingly digital world, and the place to learn about cutting-edge research in the field is the annual IEEE International Electron Devices Meeting (IEDM), to be held December 2–6, 2017 at the Hilton San Francisco Union Square hotel. Highlights for 2017 include:

- A talk on transformative electronics by Dr. Hiroshi Amano, who received the 2014 Nobel Prize in Physics along with Isamu Akasaki and Shuji Nakamura for the invention of efficient blue LEDs, which sparked a revolution in innovative, energy-saving lighting.
- The above talk is part of an exceptional slate of plenary talks to be given by some of the industry's leading figures, as listed below.
- Focus Sessions will be held on the following topics: 3D Integration and Packaging, Modeling Challenges for Neuromorphic Computing, Nanosensors for Disease Diagnostics, and Silicon Photonics: Current status and perspectives.
- A vendor exhibition will be held again, based on the success of last year's first-ever such event at the IEDM.
- The IEEE Magnetics Society will host a poster session on MRAM (magnetic RAM memories).

Each year at the IEDM, the world's best technologists in micro/nano/bioelectronics converge to participate in a technical program consisting of more than 220 presentations along with special luncheon talks and a variety of panels, special sessions, tutorials, Short Courses, IEEE/EDS award presentations and other events that highlight leading work in more diverse areas of the field than any other conference. Some of the events that will take place at this year's IEDM are:

Focus Sessions on:

- **3D Integration and Packaging**
- **Modeling Challenges for Neuromorphic Computing**
- **Nanosensors for Disease Diagnostics**
- **Silicon Photonics: Current Status and Perspectives**

90-Minute Tutorials – Saturday, Dec. 2

A program of 90-minute tutorial sessions on emerging technologies will be presented by experts in the fields, bridging the gap between textbook-level knowledge and leading-edge current research. Advance registration is recommended.

- *The Evolution of Logic Transistors Toward Low Power and High Performance IoT Applications,* Dr. Dae Won Ha, Samsung Electronics
- *Negative Capacitance Transistors,* Prof. Sayeef Salahuddin, UC Berkeley
- *Fundamental, Thermal, and Energy Limits of PCM and ReRAM,* Prof. Eric Pop, Stanford University
- *Hardware Opportunities in Cognitive Computing: Near- and Far-Term,* Dr. Geoffrey Burr, Principal Research Staff Member, IBM Research-Almaden
- *2.5D Interposers and High-Density Fanout Packaging as Enablers for Future Systems Integration,* Dr. Sundaram Venkatesh, Associate Director, Georgia Tech 3D Systems Packaging Research Center
- *Silicon Photonics for Next-Generation Optical Interconnects,* Dr. Joris Van Campenhout, Program Director Optical I/O, IMEC

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Short Courses – Sunday, Dec. 3
Short Courses provide the opportunity to learn about important areas and developments, and provide the opportunity to network with experts from around the world. Advance registration is recommended.

- *Performance Boosters and Variation Management in Sub-5 nm CMOS*, organized by Sandy Liao, Intel
- *Merged Memory-Logic Technologies and Their Applications*, organized by Kevin Zhang, TSMC

Plenary Presentations – Monday, Dec. 4

- *System Scaling Innovation for Intelligent Ubiquitous Computing*, Jack Sun, VP of R&D, TSMC
- *Driving the Future of High-Performance Computing*, Lisa Su, President & CEO, AMD
- *Energy-Efficient Computing and Sensing: From Silicon to the Cloud*, Adrian Ionescu, Professor, EPFL

Plenary Presentation – Wednesday, Dec. 6

- *Development of a Sustainable Smart Society by Transformative Electronics*, Hiroshi Amano, Professor, Nagoya University

Evening Panel Session – Tuesday evening, Dec. 5
The IEDM offers attendees an evening session where panels of experts give their views on important industry topics. Audience participation is encouraged to foster an open and vigorous exchange of ideas.

- *Who Will Lead the Industry in the Future?* Moderator: Prof. Philip Wong, Stanford University

Entrepreneurs Lunch
This popular luncheon, jointly sponsored by IEDM and IEEE EDS Women in Engineering, will be held once again. This year's speaker is Courtney Gras, Executive Director for Launch League. Event details can be found at, http://ieee-iedm.org/program/entrepreneurs-luncheon/.

Early registration is suggested, as tickets sell out fast for this crowd-pleasing event. Don't forget to sign-up for the luncheon when you register for the IEDM.

Further information about IEDM
For registration and other information, visit www.ieee-iedm.org.

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2017 IEEE Semiconductor Interface Specialists Conference (SISC)

The 48th IEEE Semiconductor Interface Specialists Conference (SISC) will be held at the Bahia Resort Hotel in San Diego, California, on **December 6–9, 2017**, immediately after the IEEE International Electron Devices Meeting (IEDM) in San Francisco. An evening Tutorial session, free to all registered SISC attendees, will be held on December 6th.

The SISC is a workshop-style conference that provides a unique forum for device engineers, materials scientists, and solid-state physicists, to openly discuss issues of common interest. Principal topics are semiconductor/insulator interfaces, the physics of insulating thin films, and the interaction among materials science, device physics, and state-of-the-art technology. Emphasis is placed on current and future nano-scale device architectures, and how interfaces between dissimilar materials and ultra-thin films affect device operation where theory, modeling/simulation, and characterization results are used to help understand the impact on device performance and reliability. The conference is held in San Diego, and meets back to back with the IEDM to encourage participation of IEDM attendees. SISC is sponsored by the IEEE Electron Devices Society.

An important goal of the conference is to provide an environment that encourages interplay between scientific and technological challenges. Oral sessions of invited and contributed talks, as well as a lively poster session, are designed to encourage discussion. Conference participants have numerous opportunities for social gatherings with renowned scientists and engineers. They also enjoy San Diego attractions including Mission Beach, Coronado Island, Sea World, La Jolla, and Old Town San Diego.

The program includes talks and poster presentations (*theory and experiment*) from all areas of semiconductor interface science and technology, including but not limited to:

- **SiO_2 and high-k gate dielectrics** on Si and their interfaces
- **Insulators on high-mobility and alternative substrates** (SiGe, Ge, III-V and III-N, SiC, etc.)
- MOS gate stacks with **metal gate electrodes**
- Stacked dielectric layers for **non-volatile memory**

- **Oxide and interface structure**, chemistry, defects, and passivation: theory and experiment
- **Electrical characterization, performance and reliability** of MOS-based devices
- **Surface cleaning technology** and impact on dielectrics and interfaces
- Dielectrics on **nanowires/-tubes** and **graphene**
- **Oxide electronics** and **multiferroics**
- **Interfaces in photovoltaics**, e.g. Si passivation
- **2D materials and devices** and their interfaces
- Interfaces in **semiconductor lighting and optical communications**
- Interfaces and surfaces in **biotechnology such as bio-sensing**

Confirmed invited speakers are:

- **Prof. Joerg Appenzeller,** Purdue U.
  2D Tunneling FET
- **Prof. Suman Datta,** Notre Dame U.
  Novel selectors and Phase FETs
- **Dr. David Ginley,** NREL
  Photovoltaic materials, Devices and interfaces by design
- **Dr. David Hemker,** LAM Research
  Enabling Continued Device Scaling: An Equipment Supplier's Perspective
- **Prof. Cheol Seong Hwang,** SNU, Korea
  Ferroelectric HfO_2 – Materials fundamentals, switching, wake-up, and applications in electronics and energy
- **Prof. Evan Reed,** Stanford U.
  Leveraging machine learning to screen 2D van der Waals materials
- **Prof. Mark Reed,** Yale U.
  Field effect transistor biosensors
- **Dr. Nirmal Ramaswamy,** Micron Technology
  Emerging memories: High density integration challenges

The **Wednesday evening Tutorial,** which is free to all registered SISC attendees, will be given by Prof. Lars Samuelson, Lund University, Sweden on *Semiconductor nanowires and their interface properties enabling photovoltaics and lighting applications.*

A unique feature of SISC is the attention paid to the poster presentations. Each author of a poster presentation has the opportunity to introduce their work orally, using two visuals, to the entire SISC audience during special poster introduction sessions. The posters are then presented during a separate poster reception on Thursday evening. A rump session organized for Friday afternoon is dedicated to a topic of current interest.

SISC is a popular conference with students, who can get immediate and candid feedback on their latest results from the experts in the field. In addition to a reduced registration fee for students, a Best Student Presentation award is given every year in memory of E.H. Nicollian, a pioneer in the exploration of the metal-oxide-semiconductor system who had a strong presence within the SISC.

The scientific content of the conference is complemented by informal events designed to encourage lively discussion and debate. A hospitality suite with complimentary drinks is available to attendees to continue their discussions on every evening of the conference. On Friday evening the conference hosts a banquet and awards ceremony, complete with the now-famous (and always riotous) limerick contest. The limericks never fail to give the conference presentations, people and events an entirely new perspective.

SISC is always a rewarding experience for specialists, students, as well as newcomers to the field. For more information about the conference, to consult its program and to register, please visit **http://www.ieeesisc.org**. We look forward to seeing you at SISC 2017!

Chris Hinkle
2017 SISC General Chair
University of Texas at Dallas, USA

Matthias Passlack
2017 SISC Program Chair
TSMC Europe, Belgium

Paul McIntyre
2017 SISC Arrangements Chair
Stanford University, USA

2018 IEEE International Memory Workshop (IMW)

The 10th International Memory Workshop (IMW) will be held at the Westin Miyako Hotel in Kyoto, Japan from May 13–16, 2018. The history of the IMW dates back to the NVSMW (Nonvolatile Semiconductor Memory Workshop) which began in 1976 and which later merged with the ICMTD (International Conference on Memory Technology and Design) to become the IMW. The IMW is sponsored by the IEEE Electron Devices Society and meets annually in May. The workshop covers all types of memory technology, is focused on advancing innovation in memory technology, and is organized in a way that provides excellent professional development and networking opportunities for attendees.

The IMW is the premier international forum for both new and seasoned technologists having diverse technical backgrounds to share and learn about the latest developments in memory technology with the global community. The scope of workshop content ranges from new memory concepts in early research to the technology drivers currently in volume production as well as emerging technologies in development. Topics include new device concepts, technology advancements, scaling and integration, circuit design and reliability, as well as emerging applications. Consistent with the increased importance of memory system architecture and integration, the workshop also includes increasing coverage of the systems in which memories are deployed and the co-evolution of memory technology along with memory systems and applications.

The IMW is the preeminent forum covering the latest developments, innovations, and evolving trends in the memory industry. Typical workshop attendance exceeds 250 attendees and the technical program begins with a full day short course given by distinguished experts that provides an excellent professional development opportunity for both new and experienced technologists. The single-track technical program spans three days and also includes an evening poster session for informal technical discussion with authors as well as a panel discussion where experts discuss and debate a current hot topic. The 2017 workshop included invited talks from industry and research leaders from Google, Samsung, Micron, IBM, Western Digital, Panasonic, Everspin, CEA LETI, and IMEC. Highlights included experts sharing their insights and perspectives on a variety of topics including the 3D NAND scaling horizon and potential successors, the latest breakthroughs in RRAM/MRAM/FRAM technology, low latency persistent memory architecture, the prospects of emerging NVM to accelerate deep learning, and the transformative impact that machine intelligence in consumer products is having on memory architecture. The technical program is organized to maximize networking opportunities and facilitate open information exchange among workshop contributors, committee members, and attendees. The program schedule includes ample time dedicated to social events including provided refreshment breaks, a workshop luncheon, and an evening banquet. This year's workshop is located near downtown Kyoto, with opportunities to explore the local temples, shrines, palaces, gardens, and museums that are part of the area's rich cultural heritage.

On behalf of the organizing committee, I cordially invite you to participate in the 2018 IMW to continue to participate in the advancement of innovation in the rapidly evolving memory industry. For additional information, including the call for papers, key dates, abstract submission instructions, registration information, and technical program details, please visit the IMW website for the latest updates: http://www.ewh.ieee.org/soc/eds/imw/. I look forward to seeing you in Kyoto this May.

Randy Koval
2018 IMW Publicity Chair
Intel

Society News

Message from EDS President-Elect

Dear Readers and EDS Members,

Fernando Guarin
EDS President-Elect

It is once again a true honor and privilege to write to you as the EDS President Elect 2016–2017. I will take this opportunity to outline some of the plans and vision for the engagement of young professionals and our involvement in humanitarian activities.

In order to remain a viable and vibrant society, EDS needs to reach out to its youngest and newest members. We must make every effort to reach out and include them with the clear realization that they represent the future of our society. It is imperative that we enhance our presence and become active in the channels that are part of their daily life. Consequently, is important for EDS to establish a strong and active presence in social media (Facebook, LinkedIn, Instagram...), not a replacement for our strong and well known communication channels, but a complementary way to engage more of our members, and reach a larger and global audience. Who better to spearhead this effort, than by engaging and leveraging our members and volunteers that are part of our Young Professionals. In my opinion one of the best tools for recruiting young members will be by enhancing and creating programs that enable our members to use their knowledge to become active participants in volunteer activities that will benefit society. We must provide a path to execute our society's mission of promoting excellence in the field of electron devices for the benefit of humanity. Any EDS members interested in devoting their time and talents to an IEEE humanitarian project will find that there are many opportunities that can be found at http://eds.ieee.org/humanitarian-programs.html

Educating and motivating young minds to engage in science and technology are one of our core programs. Since 2011 our society has taken a leadership role in outreach efforts to engage young minds starting at the elementary and High School levels through the EDS-ETC program (Engineers Demonstrating Science: an Engineer Teacher Connection). Any of our chapters wishing to visit local schools and engage their community can request kits in our EDS webpage http://eds.ieee.org/the-eds-etc-program.html. Through this initiative, we have reached over 30,000 students in all regions of the world.

The Electron Devices Society (EDS) is proud to announce that we partnered with the IEEE Foundation to establish the IEEE Electron Devices Mission Fund of the IEEE Foundation. This will be one more tool that will be available to our volunteers, by having our own mission fund currently funded with $100,000 and ready to be used to fund valuable initiatives, to enhance the humanitarian activity efforts of our members.

I look forward to your feedback on your ideas about how we can improve our society and enhance the value added that a membership to EDS will bring for you and provide the tools to make lasting contributions to society.

Fernando Guarin
EDS President-Elect
GlobalFoundries
New York, USA

Message from the Editor-in-Chief

Dear EDS Members and Readers,

Carmen M. Lilley
Editor-in-Chief
EDS Newsletter

Welcome to the October newsletter! It is a pleasure to share with you the wide array of information and articles from our chapters and members around the globe that we received for this newsletter. In particular, I was inspired by the articles demonstrating the enthusiasm of our members to share their knowledge and inspire the next generation of ED engineers around the world. These education outreach programs, conferences, and workshops show how EDS is improving access to education in communities around the world. I hope you are as inspired by these articles as I was. As always, I invite our EDS members and readers to share with me their ideas on themes they would like to appear in the newsletter and feedback on changes you see in the newsletter.

Sincerely,
Carmen M. Lilley
University of Illinois at Chicago
Editor-in Chief, EDS Newsletter
e-mail: clilley@uic.edu

Message from EDS Vice President of Publications and Products

Dear Fellow EDS Members:

Hisayo S. Momose
EDS Vice President of Publications and Products

I am very pleased to have this opportunity to update you on the latest progress and the topics in our EDS publications.

Our flagship publications, the *IEEE Transactions on Electron Devices* (T-ED), the *IEEE Electron Devices Letters* (EDL), and the *IEEE Journal of the Electron Devices Society* (J-EDS), have continued to do well over the last few years under the excellent leadership of corresponding Editor-in-Chiefs (EiCs); Giovanni Ghione for T-ED, Tsu-Jae King Liu for EDL and Mickael Ostling for J-EDS. Submitted papers are steadily increasing both in T-ED and EDL. In the case of J-EDS, they have been increasing significantly since it launched in 2013. For the three publications, we have more than one hundred editors in the Editorial Boards and many reviewers including more than three thousand Golden Reviewers last year (2016). Their outstanding contributions are really appreciated. In addition, we would like to express our sincere thanks to the EDS editorial staff and the members of Publication and Products Committee (PPC) for their continuing contributions and great support.

The publishing cycle time (Submission to e-Publication) has been improved year by year. Extremely short cycle times of 3.5 weeks and 12.7 weeks were achieved in the first half of this year for EDL and T-ED, respectively. EDL is now the fastest-turnaround IEEE journal, and T-ED also keeps the fastest of all IEEE Transactions. We are proud of these excellent results. In the case of J-EDS, the publishing cycle time is now around 11 weeks. We will work to further shorten the time as an open access (OA) journal.

Paper download statistics are important indicators for our publications, since they help to directly grasp accessing the information required by readers around the world. Based on the download statistics from IEEE Xplore, T-ED was ranked as the top eighth in all IEEE publications (from over 350 publications) last year, which had 870 thousand downloaded papers. EDL was top-ranked in the IEEE Letters publications with 530,000 downloaded papers. The total usage of J-EDS has been also growing significantly year by year, and the downloaded papers of last year became 1.5 times larger than those of 2015.

Bibliometric Indicators, such as Impact Factor (IF) and Article Influence (AF), are also known as important indexes for journals. The latest IF values are 2.61, 3.05 and 3.14 for T-ED, EDL and J-EDS, respectively. Delightfully, each value has improved compared with that of last year for the three journals. We will continue steady efforts to keep or improve the quality of the publications going forward in order to make them more attractive and to reach out to more audiences.

A few Special Issues per year have been published in T-ED and J-EDS. They are being planned on wide and high impact research areas including new developing and/or emerging areas. Reviewed Special Issues on "Power Semiconductor Devices and Smart Power IC Technologies" and "Flexible Electronics" were published with T-ED in March 2017 and May 2017, respectively. A special issue on "Vacuum Electronics" will be published with T-ED in 2018. Special issue volumes in J-EDS will also be published in 2017 and 2018, collaborating with target flagship conferences, including the European Solid-State Device Research Conference (ESSDERC) and the Electron Devices Technology and Manufacturing Conference (EDTM).

In EDL, an Editors' Picks program started last year. About six excellent papers per month are highlighted as "Editors' Picks," and available for free online within a limited time. Please use the benefit of this program to get cutting-edge valuable technical information.

J-EDS launched as the first OA journal of the Electron Devices Society in January 2013 in response to the demand for OA publishing. Recently, it has been recognized widely inside and outside of our society. Since the launch, both submissions and downloads have been increasing year by year, and the latest IF of 3.14 is a very good start, as described above. In February 2017, we successfully completed the first review for J-EDS by the IEEE Periodicals Review and Advisory Committee (PRAC). We obtained very positive feedback from PRAC regarding the issues of timeliness and quality. For the success of our journal at the first stage, we would like to especially thank Renuka P. Jindal (First EiC) and Mikael Ostling (Current EiC) for their outstanding leadership. In accordance with members' need, we will continue to strategically work and go forward to make J-EDS one of the top-tiered topical OA publications within competing OA publications on device technology.

Finally, we report the latest progress of our co-sponsored publications briefly. EDS co-sponsors several leading journals, including the *IEEE Journal of Photovoltaics* (J-PV), the *IEEE Transactions on Device and Materials Reliability* (T-DMR), the *IEEE Transactions on Semiconductor Manufacturing* (T-SM), the *IEEE Journal of Lightwave Technology* (J-LT), and the *IEEE Journal of Microelectromechanical Systems* (J-MEMS). The submissions of these five journals have been holding steady in recent years. The total usage statistics from IEEE *Xplore* downloads are

also steady for all the journals. J-LT had around 570,000 downloaded papers last year, and was ranked among the thirtieth in all IEEE publications. That of J-PV has been increasing recently, reflecting the readers' interests.

We hope that all researchers in the Electron Device area consider publishing devices-related articles first in our EDS publications. We would like to increase our flexibly to meet members' need and provide better service to the community. In order to improve our journals further, your feedback is really appreciated. If you have any suggestions and comments, please contact me by email (h.s.momose@ieee.org) or Ms. Marlene James, Supervisor EDS Publications (m.james@ieee.org).

Sincerely,
Hisayo S. Momose
EDS Vice President of Publications and Products
e-mail: h.s.momose@ieee.org

EDS Photovoltaic Devices Technical Committee Report

The EDS Photovoltaic Devices Technical Committee (TC) has the charter to identify new emerging areas in photovoltaic (PV) devices, and to promote activities in PV among EDS members. The TC consists of 12 members: Armin Aberle, Tim Anderson, Paul Basore, Richard Corkish, Sonia Diniz, Ned Ekins-Daukes, Larry Kazmerski, Hassan Qasem, Angele Reinders, Charles Surya, Sunit Tyagi and Juzer Vasi (Chair). The Committee had a face-to-face meeting on June 28, 2017 during the 44th IEEE Photovoltaic Specialists Conference (PVSC) in Washington DC, which was held from June 25–30, 2017. All members of the Committee except 3 were able to attend this meeting. EDS President, Samar Saha, was also present as he was attending the PVSC.

To start off the meeting, Samar Saha gave a brief overview of EDS and the mandate of Technical Committees. The Committee then discussed various issues related to photovoltaics and what the TC could do to leverage the technical excellence of EDS to impact photovoltaics research and deployment worldwide. Some of the suggestions are:

- The TC can play an important role in disseminating technical information about PV globally, especially to industry in the manufacturing countries, where IEEE has a strong presence through its Sections and Chapters.

Attendees at the meeting of Photovoltaic Devices TC meeting at PVSC in Washington, D.C., on June 28, 2017. (L to R): Angele Reinders, Larry Kazmerski, Sunit Tyagi, Samar Saha, Richard Corkish, Sonia Diniz, Charles Surya, Tim Anderson, Paul Basore, Juzer Vasi

- The TC can encourage EDS chapters to conduct the EDS signature 'Mini-Colloquia' with a focus on new developments in photovoltaics.
- The TC can solicit a Review paper on some of the important new developments in PV devices, which could be published jointly in *IEEE Transactions on Electron Devices* (TED) and *IEEE Journal of Photovoltaics* (JPV). This would have the benefit of bringing such developments to the attention of a wider electron devices community.

It was decided that the above suggestions would be taken up by the committee and pursued further. The Committee also discussed the recommendation from Carmen M. Lilley, Editor-in-Chief of the EDS Newsletter, that a 'Technical Brief' article giving the Highlights of the PVSC conference be published in the Newsletter on an annual basis. This article would be similar to the very successful IEDM Highlights which appears annually. This suggestion was agreed to, and Angele Reinders, who is also the 2017 PVSC Conference Chair, agreed to follow up on this.

The Committee also agreed that the TC would meet every year while attending IEEE PVSC, since most members are likely to attend this conference. Accordingly, the next meeting of the Photovoltaic Devices TC is scheduled to be held in Hawaii in June 2018.

EDS members who would like to offer suggestions to the TC are most welcome to write to the Chair, Juzer Vasi, at j.vasi@ieee.org.

Juzer Vasi
Chair, EDS Photovoltaic Devices Technical Committee
Indian Institute of Technology Bombay

Message from Leda Lunardi, EDS Women in Engineering Liaison

Leda Lunardi
EDS WIE Liaison

I have been representing the EDS as the IEEE Women in Engineering Liaison since January 2016. One myth that exists is that WIE is only for women, when actually today WIE has more than 20,000 members from which 1/3 identify themselves as males. This may be related to the lack of information around the formation of WIE, which started in 1993 as an ad-hoc committee to address the increase in IEEE membership that identifies themselves as females (about 8% of the total IEEE members). An interest in having an umbrella organization for women with the rapidly number of members joining WIE prompted the IEEE board to pass a resolution for letting the group start collecting membership dues and having separate representation at the board of directors without voting privileges. Some geographic regions have a larger percentage of WIE members than other areas, (Regions 1–8 have the lowest fraction of the total members that are WIE members, while Regions 9–10 have the largest participation). The majority of the WIE members are students (undergraduate and graduate) that benefit from creating a professional network and receiving different perspectives for their technical careers in engineering and science.

As the EDS liaison, I participate in monthly conference calls with all the other technical societies and councils representatives and on alternate months with the WIE executive committee.

Some of us volunteer for WIE activities including the WIE newsletter, awards committees, workshops, technical committees and outreach.

WIE has sponsored several technical leadership career development projects that began in Silicon Valley and more recently expanded internationally. These events are organized in different geographical areas in conjunction with IEEE technical conferences or meetings, and co-sponsored by IEEE regions.

Last year in November 2016, I attended the WIE leadership summit sponsored by Region 3 in Atlanta, Georgia: tailored to attract Georgia Tech and regional engineering students. It was well attended by local area industry, defense contractors and professionals.

With the input of the liaisons, the WIE executive committee is starting to compile the best practices that exist around the IEEE technical societies related to the involvement of women and underrepresented minorities in committees and technical conferences.

Consider in joining IEEE WIE: the membership is free for students, graduate student members and life members, while for IEEE member dues are US$25 annually.

Leda Lunardi
EDS Women in Engineering Liaison
North Carolina State University
Raleigh, NC, USA

EDS/Women in Engineering Co-sponsor Entrepreneur Luncheon at IEDM

Courtney Gras
Invited Speaker

At the 63rd IEEE International Electron Devices Meeting, the Entrepreneur Luncheon will be held on Tuesday, December 6, 2017, at the San Francisco Hilton. This event sponsored by IEDM and EDS/Women in Engineering with Leda Lunardi as moderator, will feature Courtney Gras, an electrical engineer who started her entrepreneurial career while still an undergraduate student and the co-founder of the Akron-based Design Flux Technologies, a clean energy startup.

She discovered a passion for building startup communities and helping technology-focused companies meet their goals. Presently she is the Executive Director for Launch League, an Akron-based nonprofit focused on developing a strong startup ecosystem in NE Ohio with her work as a business development consultant for local technology companies.

In 2016 she was named, while serving as Chief Operations Officer, a "Forbes 30 under 30". She has also been named to the "Top 40 under 40" in Cleantech by Midwest Energy News and one of Crain's "Twenty in their 20s." More recently on August 26, 2017 she has been featured in TEDx Talks with "Why Success Will Keep You Moving."

Leda Lunardi
EDS Women in Engineering Liaison

EDS Members Recently Elected to IEEE Senior Member Grade

Pierre-Jean Alet
Roger Booth
Rongming Chu
Werner Drexel
Abel Garcia
Stephen Heinrich-Barna
Haslina Jaafar*
Carlos Leal Saballos
Matthew Marinella
Marco Munguia
Ken Nishimura
Taiji Noda
Rebecca Peterson
C. Pinzone
Angele Reinders
C. Selvakumar
Oscar Somarriba
Chan Tan
Miaomiao Wang
Ahmad Sabirin Zoolfakar*

Thank you to the EDS members who remembered to designate the Electron Devices Society as their nominating entity!
Indicated with an asterisk(*).

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request, a letter will be sent to employers, recognizing this new status. For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application after signing in with your IEEE account: https://www.ieee.org/membership_services/membership/senior/application/index.html.

2016 EDS PAUL RAPPAPORT AWARD

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. Every year, the Society confers its prestigious Paul Rappaport Award to the best paper published in the *IEEE Transactions on Electron Devices*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The winning paper was selected from over 740 articles that were published in 2016. The winning paper is titled *"A Color-Tunable Polychromatic Organic-Light-Emitting-Diode Device with Low Resistive Intermediate Electrode for Roll-to-Roll Manufacturing."* This paper, published in the January 2016 issue of the *IEEE Transactions on Electron Devices*, was authored by Takatoshi Tsujimura, Takeshi Hakii and Suguru Noda.

The award will be presented at the plenary session of the IEEE International Electron Devices Meeting to be held on December 4, 2017, in San Francisco, California. In addition to the award certificate, the authors will receive a check for USD$2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of the authors follow.

Takatoshi Tsujimura was selected as "10 best engineers/researcher in 10 best Japanese companies" by Nikkei Electronics Magazine. He received the SID Special Recognition Award and SID Fellow Award for his development of OLED TV technology, which has become an industry standard. He is currently a Konica Minolta Fellow and is a CTO of Konica Minolta Pioneer OLED.

Takeshi Hakii has been working with Konica Minolta since 1995. He is responsible for next generation technology for flexible OLED. He received a bachelor's degree in

Applied Chemistry in 1995 from Waseda University, Tokyo, Japan. He has developed many products such as OLED lighting, wearable displays and electronic papers.

Suguru Noda is a professor at the Department of Applied Chemistry, Waseda University, Japan. He has conducted research in the field of materials processing, especially thin films by chemical and physical vapor deposition methods. He is recently focusing on practical production of carbon and silicon nanomaterials for energy and electronic applications.

Hisayo S. Momose
EDS Vice President of Publications and Products
h.s.momose@ieee.org

2016 EDS George E. Smith Award

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. The George E. Smith Award was established in 2002 to recognize the best paper appearing in a fast turnaround archival publication of EDS, targeted to the *IEEE Electron Device Letters*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The paper winning the 2016 George E. Smith Award was selected from over 390 articles that were published in 2016. The paper is entitled, "*An Experimental Demonstration of GaN CMOS Technology.*" This paper appeared in the March 2016 issue of the *IEEE Electron Device Letters* and was authored by Rongmin Chu, Yu Cao, Mary Chen, Ray Li, and Daniel Zehnder.

The award will be presented at the plenary session of the IEEE International Electron Devices Meeting to be held on December 4, 2017, in San Francisco, California. In addition to the award certificate, the authors will receive a check for USD$2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of the authors follow.

Rongming Chu received his PhD at UC-Santa Barbara, working on GaN microwave transistors. After finishing his degree in 2008, he spent two years at Transphorm, Inc., then a

start-up company commercializing GaN power switching technology. He joined HRL Laboratories in 2010 as a Research Staff responsible for GaN power device technology development, and became a Senior Research Staff in 2014. His research at HRL includes GaN-on-Si lateral power transistors, GaN-on-GaN vertical power devices, and more recently GaN CMOS IC. He served on the technical program committees of the IEEE Workshop on Wide Bandgap Power Device and Applications, the IEEE Lester Eastman Conference, and the Asia-Pacific Workshop on Wide Bandgap Semiconductors.

Yu Cao received the PhD degree in Electrical Engineering at the University of Notre Dame. He is currently a research staff scientist at HRL Laboratories, working on GaN epitaxy and devices. As a senior member of IEEE, he has authored 3 books/chapters, over 120 peer-reviewed journal and conference papers.

Mary Chen received her B.S. in physics at Mount Holyoke College with magna cum laude in 1983, and her Ph.D. in electrical engineering from Cornell in 1988. She has experience with compound semiconductor devices in several material systems for high speed and high power MMIC applications, and high-speed digital IC applications. She is currently with Microelectronics Laboratory of HRL Laboratories LLC.

Ray Li is an IEEE member. He received his Ph.D. in Chemical Engineering from University of California, Riverside. He developed the processes for different generations of lateral and vertical GaN devices at HRL. He has authored and co-authored more than 30 publications and patents.

Daniel Zehnder received the electrical engineering degree from the Gewerbliche Berufsschule Biel, Switzerland, in 1992. He joined HRL Laboratories in 2004 as a Senior R&D Specialist. His experience is on-wafer characterization of power electronic devices and high speed mixed signal circuits, and the design of Printed Circuit Boards for device verification.

Hisayo S. Momose
EDS Vice President of Publications and Products
h.s.momose@ieee.org

Call for Nominations

IEEE EDS William R. Cherry Award

The IEEE Electron Devices Society invites the submission of nominations for the 2018 William R. Cherry Award.

This award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry award was instituted in 1980, shortly after his death. The purpose of the award is to recognize an individual engineer or scientist who devoted a part of their professional life to the advancement of the science and technology of photovoltaic energy conversion.

The award consists of a plaque, monetary award, recognition at the PVSC Opening Ceremony and a dedicated Cherry Award Talk during the Opening Ceremony. A reception is also held in honor of the Cherry Award winner during the PVSC.

Nominate:
William R. Cherry Award online nomination form:
https://ieeeforms.wufoo.com/forms/eds-william-r-cherry-award-nomination-form/

Submission Deadline:
January 31, 2018

For more information:
http://www.ieee-pvsc.org/PVSC45/awards-cherry.php

ORGANIZING IEEE EDS STEM WORKSHOPS FOR KIDS TO BUILD ELECTRONIC CIRCUITS

PREPARED BY SANG LAM AND MANSUN CHAN
DEPARTMENT OF ELECTRONIC & COMPUTER ENGINEERING,
HONG KONG UNIVERSITY OF SCIENCE & TECHNOLOGY (HKUST)

Introduction

Advancements of electron devices have revolutionized our modern world [1], both in terms of our lifestyle and industrial manufacturing activities. While electronic technologies are indispensable in our everyday life, young students and children do not have many chances to acquire the skill of circuit construction until a very late stage of their education. With the belief that electronic projects can be introduced at a much earlier stage in our education system, EDS and the ED/SSC Hong Kong ED/SSC Chapter have initiated a number of workshops and exploration camps to let students as young as 10 years old explore electronic circuits by building interesting electronics [2] such as a running light indicator, an electronic piano, an infrared detector, etc. In this article, we share our experience and knowledge in organizing such educational activities with the IEEE EDS community, and especially for those interested in organizing similar activities in their local communities.

Motivation

Hosting electronic circuit exploration workshops can achieve multiple goals. The hands-on reverse engineering approach is expected to arouse students' interest in electronics without in-depth understanding that usually takes much longer time to acquire. Once the students develop their interest, they will pursue the required knowledge without much guidance in this information-rich generation [3]. In organizing such workshops, university students are recruited as helpers.

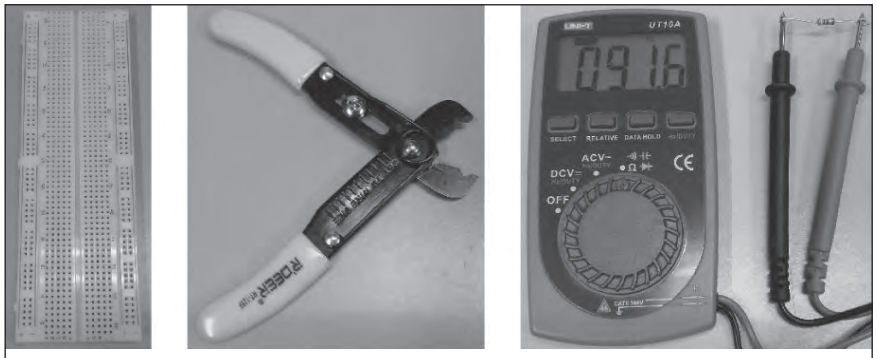

Fig. 1. Basic tools required for electronic circuit construction: (a) a breadboard, (b) a wire stripper and (c) a digital multimeter

Through serving as student helpers to explain the process of circuit construction to schoolchildren, they can practice their organization skills and develop their abilities in communicating technical ideas to a non-technical audience. By organizing these events, the organizers as well as the event sponsors can have increased visibility among schools and even the general public. The workshop can also reach out to parents to do projects together with their kids outside the workshops. Parents spending time with their children on doing something together with fun is always desirable.

Resources

The electronic circuit construction requires only very basic tools (such as a breadboard, a wire stripper and a multimeter) (Fig. 1) and components (e.g. resistors, capacitors, LEDs, chipsets etc.) (Fig. 2) which are all readily available at affordable prices. As a result, the circuit construction workshop can be delivered anywhere with a desk at school or at home [3]–[5]. In addition, ordinary batteries are used and the voltage is low enough not to hurt a person, though some sensitive electronic devices may be damaged by circuit mistakes. No soldering iron is needed as the electronic circuits are built on a prototyping breadboard (Fig. 1a).

General Practices

In delivering such electronic circuit construction workshops, only essential physical concepts are taught. Whenever possible, understandable analogies using daily life examples are used to explain concepts. The theory discussion of electronics is kept minimal when delivering the workshops. Neither prior knowledge or skills of electronics are assumed for the workshop. As for the mathematics requirement, simple arithmetic (addition, subtraction, multiplication, division) is sufficient for building the electronic circuits in the workshop.

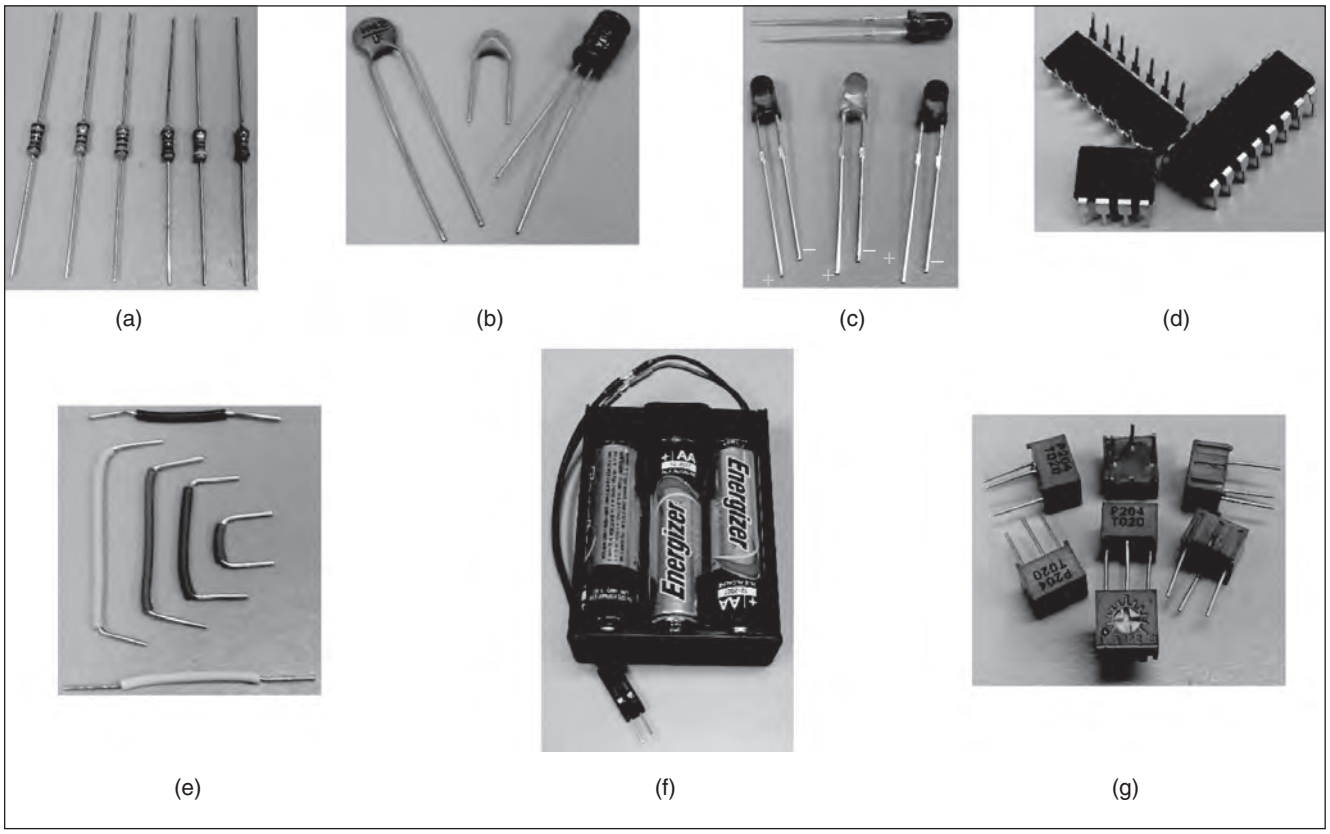

Fig. 2. Inexpensive components readily available for electronic circuit construction: (a) resistors, (b) capacitors, (c) LEDs, (d) chipsets, (e) wires, (f) batteries inside a battery box and (g) variable resistors

Delivering the Workshop – General Skills

The workshop can start with a demonstration of how to use a wire stripper (Fig. 1b) as the basic tool. Since the hands-on approach is the essence of the workshop, participants should be given the first task of cutting and stripping wires in plastic coatings (Fig. 2e). It is then natural to explain about electrical wires. A daily life analogy of water pipes can be used. When explaining about electrical wires, the two important quantities in electronic engineering, namely current and voltage, should be introduced. The corresponding units of current and voltage need to be included as well. With the concept of voltage introduced, a battery (Fig. 2f) can be depicted as a voltage source or generator. Based on the concepts of voltage and current, the concept of resistance can then be explained. The daily life example of water flow can be used to illustrate the idea of resistance. After explaining about resistance, it is natural to proceed to the introduction of resistors together with the color code of discrete component resistors (Fig. 2a). The second hands-on task would be reading the color code of a few resistors to figure out the resistance. Afterwards, the use of a multimeter (Fig. 1c) for measurements of current, voltage and resistance can be taught. With basic demonstrations, students should be able to learn easily how to use the multimeter (Fig. 1c). The third hands-on task would be the measurements of the resistors and checking the resistance against the values read from the color code.

The next key apparatus to introduce is the breadboard, shown in Fig. 1a, for use as a handy circuit board for quick prototyping of electronic circuits. The properties of the breadboard should be carefully explained, especially the electrical connections of the pin holes along different rows and columns. As the fourth hands-on task, a multimeter (Fig. 1c) can be used to verify the electrical connections along a row and a column and the electrical isolation between different rows. Without explaining the theory of operation, a light-emitting diode (LED) (Fig. 2c) can be introduced as a light indicator which works only when current flows in one direction but not the other. Students should be taught how to identify the two different electrodes of an LED (Fig. 2c). With the positive and negative electrodes of the LED explained, the use of a battery box (Fig. 2d), which has positive and negative terminals as well as a switch to turn on the voltage, can then be described. This leads to the fifth hands-on task in using a battery box, an LED and a resistor to construct a simple circuit of

Table 1. List of components, electronic engineering concepts, tools and hands-on tasks for an introductory session on electronic circuit exploration			
Component	**Engineering Concept**	**Tool**	**Hands-on Task**
Electrical wires	Current & voltage and the corresponding units (ampere & volt)	Wire stripper	Cutting & stripping wires
Resistors	Resistance		Reading the resistance values from the color codes of resistors
	DC measurement	Multimeter	Measurements of the resistance of resistors
Breadboard		Multimeter	Verification of the electrical connections of a breadboard
Light-emitting diode (LED)	Unidirectional current flow		
Battery box	DC power source; distinguishing positive & negative terminals		Circuit construction of a simple light indicator
Variable resistor			Circuit construction of a simple light indicator with adjustable brightness

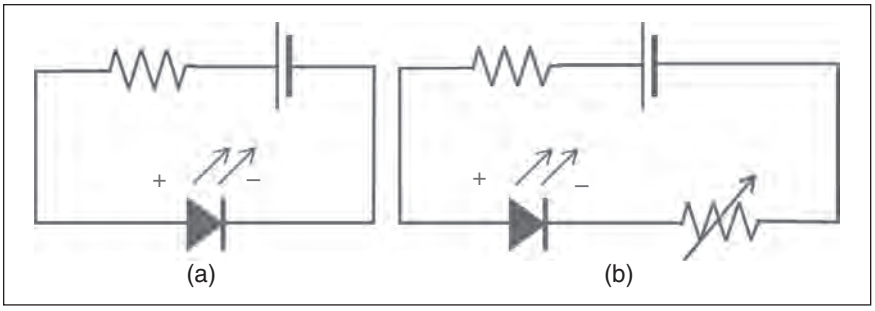

Fig. 3. Basic LED indicator circuit for hands-on circuit construction tasks with noticeable visual effects when working (a) with fixed brightness; (b) with a variable resistor for adjusting the resistance and hence the brightness

an LED light indicator (Fig. 3a). The last component to be introduced in the first session of the workshop is the variable resistor (Fig. 2g) which allows the adjustment of the resistance. Quick demonstrations about the variable resistance measured by a digital multimeter (Fig. 1c) can be given. The sixth and final hands-on task is simply modifying the circuit in the fifth task by including a variable resistor (Fig. 3b). By adjusting the variable resistor, the brightness of the LED can be varied. The visual effect is easily noticeable to tell whether the circuit works or not. A minor reminder here is that some variable resistors have three pins. Wrong connections of the pins would give no change of the resistance and thus having no brightness change of the LED. Table 1 gives a summary of the components, electronic engineering concepts, tools and the hands-on tasks taught in the first session of the electronic circuit exploration workshop. It can be seen that the delivery of such electronic circuit exploration workshop is both highly educational and of much fun.

In the next issue of the newsletter, we will move on to the first project involving an integrated circuit to generate a running light. The teaching material can be downloaded from the education section of the EDS website (http://eds.ieee.org/ieee-exploration-camp.html).

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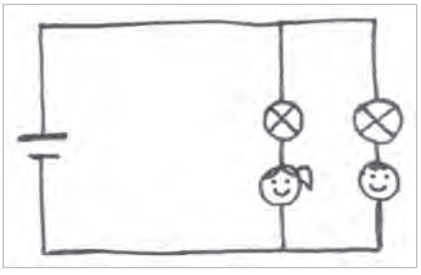
EDS-ETC in Silicon Valley (ED Santa Clara Valley/ San Francisco Chapter)

By Sachin Sonkusale

Palo Alto in Silicon Valley is the land of innovation and engineering. However, across the freeway exists East Palo Alto, an underserved community. Here, many children do not have the opportunity or awareness to explore STEM. The lack of mentors and role models has prevented many children from reaching a higher educational goal. It is a city in need of the EDS-ETC Program.

The ED Santa Clara Valley Chapter sponsored two one-week summer camps at the East Palo Alto Library to teach young children (6–12 years old) the basics of circuits and electricity. The course was taught by Uma Bahl, ED SCV Chapter volunteer, who designed a fun program using Snap Circuits kits provided by the EDS-ETC program. Ten children attended the program each week, learning by a 'hands-on' approach supplemented with classroom instruction. The East Palo Alto Library staff organized student enrollment and classroom facilities in the library, which helped the camp run efficiently.

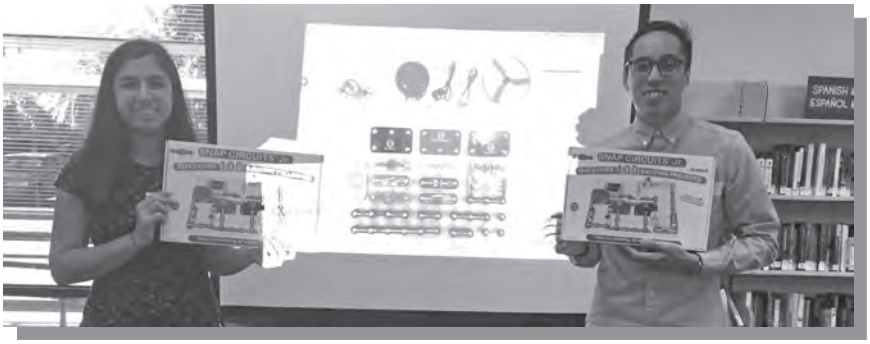


Elle and Elliot go through a parallel circuit (in parallel!)

Uma taught the lessons in a fun, interactive, story-like format. The students enjoyed learning concepts like voltage, resistance, and current through the character "Elle the Electron" and her brother Elliot. In addition, they learned what makes up a circuit, parallel vs. series circuits, how to avoid short circuits and what makes a good conductor. The kids had fun trying all the different projects in the project book and even ended up constructing their own ideas. They also learned how to use a DMM (digital multimeter) and the foundations of loop equations by measuring and summing up the potential differences in a circuit. At the end of the week, students with perfect attendance were able to take a kit home. Some of them even took the kits to their grandparents' house and taught them how to make a circuit. The camp was so successful that some children volunteered to help Uma run and grow the program next year.

The ED SCV chapter donated the take home kits for the first week, and the East Palo Alto Library donated

Uma Bahl, IEEE SCV EDS Chapter volunteer, with her TA (back row) and class of ten students. Each hardworking student got a certificate of completion and a Snap Circuits kit to take home



Uma Bahl stands with Kenny Ocana (East Palo Alto Summer Camp Coordinator)

Instruction consisted of a "hands-on" approach supplemented by classroom instruction

the kits for the second week. Giving the kits made a huge difference as the children's interest and education continues long after the camp is over.

The parents also had very positive comments. One mother said she was not able to send her son to a similar camp due to the expense. Another mother said she would never have realized that her daughter likes circuits if it had not been for this camp. The kids were very enthusiastic, and this camp has certainly given them the exposure to consider electrical and electronic engineering as a career.

There is an engineer in all of us, and the EDS-ETC program completes the circuit with this summer camp to help us discover it. For more information on this chapter's program, contact Sachin, ED SCV Chapter Chair, at Sachin.Sonkusale@ieee.org.

~ Kyle Montgomery, Editor

ED Sri Jayachamarajendra College of Engineering Student Branch Chapter, Mysore, India

By S. B. Rudraswamy

Vacation Project Mania (VPM) is an annual workshop, which is conducted by the EDS community of IEEE SJCE for the past seven years. This two-week workshop aims at enhancing the practical skills of students and encouraging them to take up real-time projects that bring out the problem solvers' trait in the budding engineers. The workshop was conducted June 1–12, 2017, with a total number of 110 participants this year. VPM has two phases throughout the workshop. The first phase deals with analog electronics and intends to make students aware of practical aspects of circuit design, and the second phase deals with

Participants enthusiastically solving the 'Hackathon' tasks

the microcontrollers. Students were introduced to programs that can blink LEDs, analog to digital converters (ADC) interfacing of LCD (liquid crystal display), interrupts, timer and pulse width modulation (PWM) with the ATmega16 VPM 8.0, and ended with a "HACKATHON", wherein a set of problems were given to the participants and they were asked to debug.

~ Manoj Saxena, Editor

EDS-ETC Program at ED University of Calcutta Student Branch Chapter

By Sarmista Sengupta and Soumya Pandit

On March 21st, the ED University of Calcutta Student Branch Chapter and the IEEE WIE Calcutta Section, jointly organized a hands-on training session for Elenco Snap Circuits kits as part of the Engineers Demonstrating Science: an Engineer Teacher Connection (EDS-ETC) program. The program was conducted at the Institute of Radio Physics and Electronics, University of Calcutta and 20 students of Victoria Institution School from class IX and X participated. At first, there was a tutorial session about the basics of digital circuits, then students were allotted with a hands-on training session with the Snap Circuits kits. The entire program was conducted by M.Tech. and PhD students.

~ Manoj Saxena, Editor

Demonstration of the Snap Circuits kits

Volunteers Needed for IEEE Humanitarian Programs

In recent years, IEEE has placed great emphasis on Humanitarian Technology Activities as part of its strategic efforts to advance technology for the good of humanity. A program called Special Interest Group on Humanitarian Technology (SIGHT) was created to further these efforts.

EDS members interested in devoting their time and talents to an IEEE humanitarian project will find that there are many opportunities.

We encourage current EDS chapters to form a SIGHT group and qualify for the $250 seed funding.

Should you submit a proposal to start a new SIGHT group and participate in any of the IEEE humanitarian programs listed below, please make sure to indicate the Electron Devices Society as your Operating Unit (OU).

For more details on this program, visit the IEEE SIGHT webpage: http://www.ieee.org/special_interest_group_on_humanitarian_technology.html.

Chapter News

MQs, DLs and Conference Reports

EDS Distinguished Lecturer Mini-Colloquium

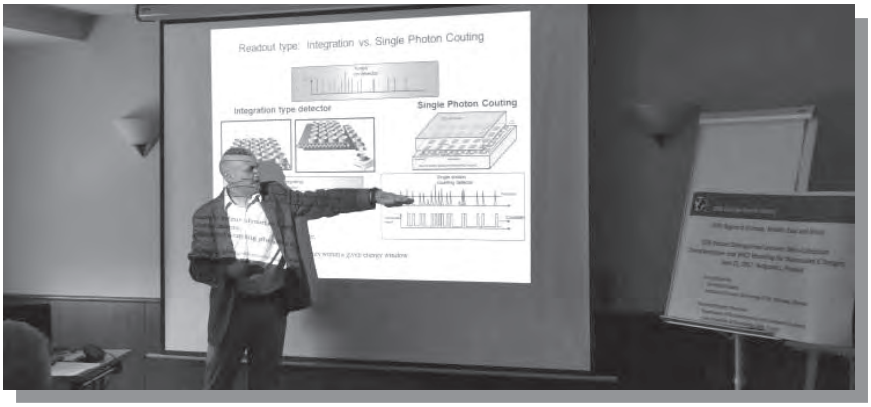
"Characterization and SPICE Modeling for Nanoscaled IC Designs"

By Andrzej Rybarczyk and Daniel Tomaszewski

The EDS Distinguished Lecturer Mini-Colloquium *"Characterization and SPICE Modeling for Nanoscaled IC Designs"* was held in Bydgoszcz, June 21, 2017. It was organized by the ED Poland Chapter, and Institute of Electron Technology (ITE), Warsaw, Poland. The technical support for the seminar was provided by the Department of Microelectronics and Computer Science (DMCS), Lodz University of Technology. Support from MOS-AK Research Group (www.mos-ak.org) is also acknowledged.

The Mini-Colloquium was dedicated to the students, engineers and researchers working in the field of silicon-based micro- and nanoelectronics: technology/device modeling and characterization, and device/integrated circuit design. The program of the full-day event consisted of the following presentations:

- *"Advanced Silicon photonics device and process technology of photonic integrated circuits for optical interconnect"* by Dr. Tohru Mogami (EDS Distinguished Lecturer), Photonics Electronics Technology Research Association (PETRA), Tsukuba, Japan (work partly supported by NEDO).



Lecture of Prof. Paweł Gryboś

Participants of the Mini-Colloquium

Abstract: Optical interconnect is an important technology for wide-band and large-capacity data communications. Photonics devices have so far been fabricated using non-Si materials. This has made device integration difficult. Recently, Si photonics technology has emerged. Silicon photonics based on Si CMOS technology is a key to produce integrated photonic chips. It has advantages of stable device integration on a chip and low-cost with high-speed and large-capacity performance. In the presentation, the silicon photonics technology for optical interconnects was address from the viewpoint of optical device theory and process techniques. Furthermore, the recent advances in silicon photonics by PETRA and other companies were introduced and perspectives of the future silicon photonics technology were discussed for advanced photonic integrated circuits.

- *"Photoelectric characterization of the MIS system. Theory, our contributions and recent advances"* by Prof. Henryk Przewłocki (EDS Distinguished Lecturer), Institute of Electron Technology, Warsaw, Poland.

Abstract: The "classical" theory of the MIS system photoelectric characteristics was presented. Weak points of

this theory were pointed out by comparing its results with experimental data. In particular, it was shown that the theory did not properly predict the photocurrent vs. voltage characteristics of MIS structures at weak electric fields in the insulator. Physical phenomena responsible for that were explained and appropriate corrections to the theory were presented. It was also shown that the classical theory did not account for differences in characteristics of the MIS structures with n- or p-type substrates. Experimental proof of these differences was shown and explained. Appropriate corrections to the theory were discussed. Finally, application results of the novel Graphene-Insulator-Semiconductor (GIS) test structures in photoelectric characterization of semiconductor devices were presented and their advantages demonstrated.

- *"An outline of Qucs-S compact device modelling: History and capabilities"* in two parts: *"Equation-Defined Device (EDD) modelling to Verilog-A module synthesis"* and *"XSPICE Code Models; basic properties to model synthesis, and beyond"* by Prof. Mike Brinson of London Metropolitan University, UK.

Abstract: Almost ten years ago, the Qucs Development Team started the process of adding compact device modelling features to the widely used Qucs circuit simulator. In 2017, the first stable version of the multi-simulator version of Qucs, called Qucs-S, was released. This GPL software package provides users with an extensive range of simulation and modelling tools, including (1) Ngspice, SPICE OPUS and Xyce and (2) subcircuits, nonlinear EDD, SPICE B style sources, Verilog-A modules, XSPICE Code Models, SPICE netlist synthesizers, Verilog-A, module and XSPICE Code Model synthesizers. The properties and use of these simulation modelling tools were introduced and their application described with a series of semiconductor device models.

- *"Noise and mismatch minimization in the design of multichannel integrated circuits"* by Prof. Paweł Gryboś, AGH University of Science and Technology, Krakow, Poland.
- *"ASCENT: Access to European Nanoelectronics Infrastructure"* by Prof. Jim Greer, ASCENT Program Coordinator, and Nicolás Cordero , both Tyndall National Institute (Ireland).

Abstract: ASCENT (http://www.ascent.network/) is a European Infrastructure access program, which brings together IMEC (Belgium), Leti (France) and Tyndall (Ireland). ASCENT provides fast and easy access to the world's most advanced CMOS nanoelectronics data and test structures in Europe's leading nanofabrication research institutes. ASCENT offers 14 nm CMOS (FDSOI and finFET) device data, nanoscale test chips and electrical/physical characterization facilities. ASCENT enables Europe's world-leading TCAD and compact modeling community to perform the systematic studies that are required to develop nanoscale design methodologies. As part of the ASCENT offer, the TCAD and compact modelling community has OPEN ACCESS to 14 nm PDKs and electrical characterization data through the ASCENT Virtual Access (VA) service.

Nearly twenty researchers and students attended the mini-colloquium. During the sessions and the breaks interesting discussions regarding the talks were triggered. A warm atmosphere at the event is worth mentioning.

24th International Conference on Mixed Design of Integrated Circuits and Systems – MIXDES 2017

On June 22–24, 2017, the annual International Conference MIXDES 2017 was held in Bydgoszcz, Poland. The event was organized by the Lodz University of Technology and the Warsaw University of Technology. The conference was co-sponsored by the IEEE Poland Section ED and CAS Societies, Polish Academy of Sciences (Section of Microelectronics and Electron Technology), and Commission of Electronics and Photonics of Polish National Committee of International Union of Radio Science – URSI.

The three-day conference program consisted of 113 talks, included invited speeches, as well as oral and poster presentations submitted from 23 countries.

In addition to the regular program, there were five invited speakers with their talks titled below:

- *Digitally-Assisted Analog-to-Digital Converters in Deep-Nanoscale CMOS*
  João Goes (Universidade Nova de Lisboa, Portugal)
- *Emerging Sigma-Delta Modulation Techniques for an Efficient Digitization in the Internet of Things*
  Jose M. de la Rosa (Universidad de Sevilla, Spain)
- *High-Performance Silicon Photonics Platform for Low-Power Photonic Integrated Circuits* Tohru Mogami (PETRA, Japan)
- *Introduction of Analog Front End IC Used in Sensing System*
  Yoichi Shimeno (New Japan Radio Co., Ltd., Japan)
- *The Future of CMOS: More Moore or the Next Big Thing?*

Attendees of MIXDES 2017

Wiesław Kuźmicz (Warsaw University of Technology, Poland)

The sessions also included presentations in four special sessions:

- *Compact Modeling for Characterization and Design of CMOS ICs* organized by D. Tomaszewski (Institute of Electron Technology, Poland) and W. Grabiński (GMC Suisse, Switzerland)
- *New Trend of Analog Systems* organized by The Research Committee on Electronic Circuits of the Institute of Electrical Engineers of Japan (IEEJ)
- *Methods for Human Balance Disorders Assessment and Rehabilitation* organized by Lodz University of Technology, Poland
- *xTCA for Instrumentation* organized by S. Simrock (ITER, France) and D. Makowski (Lodz University of Technology, Poland)

The authors of selected papers received *Best Paper Award* diplomas and the Polish Section of the IEEE ED Chapter presented the Young Scientist Paper Award to Weronika Zubrzycka for the paper entitled "*Biasing Potentials Monitoring Circuit for Multichannel Radiation Imaging ASIC In-system Diagnostics*."

The 2018 MIXDES Conference will take place in Gdynia. The Preliminary Call for Papers is available at http://www.mixdes.org/downloads/call2018.pdf. More information about past and upcoming MIXDES Conferences can be found at http://www.mixdes.org.

~ Mariusz Orlikowski, Editor

EDS Mini Colloquium at ED Tainan Chapter

By Wen-Kuan Yeh

The ED Tainan Chapter organized a Mini Colloquium at National Nano Device Laboratories (NDL), Hsin-Chu, Taiwan on April 27, 2017. This MQ focused on "Emerging Materials and Technology for Advanced Nano Device." The following seven speakers were invited to give EDS Distinguished Lectures:

- "A perspective of recent advances in graphene-based research" by Dr. Nai-Chang Yeh, Professor of Physics, California Institute of Technology, USA
- "On the Lanthanum-based Subnanometer EOT Gate Dielectric Films" by Dr. Hei Wong, Professor of Department of Electronic Engineering at City University of Hong Kong, Hong-Kong

Speakers for IEEE MQ 2017 (left to right), Akinwande Deji, Nai-Chang Yeh, Wen-Kuan Yeh, Steve S. Chung, Hei Wong, Jen-Inn Chyi, Shoou-Jinn Chang, and Chee-Wee Liu

- "2D Emerging Devices: From ordinary to extraordinary" by Dr. Akinwande Deji, Professor of Department of Electrical and Computer Engineering, The University of Texas at Austin, USA
- "High mobility transsistors using strained Si, SiGe, Ge, and Ge

Sn channels" by Dr. Chee-Wee Liu, Professor of Department of Electrical Engineering, National Taiwan University, Taiwan

- "A Logic CMOS Compatible Single-transistor NVM Feasible for Embedded Applications" by Dr. Steve S. Chung, Chair Professor, National Chiao Tung University, Taiwan
- "Technology challenges of GaN-based electronic devices for power and RF applications." by Dr. Jen-Inn Chyi, Chair professor of Department of Electrical Engineering, National Central University, Taiwan
- "Enhanced conversion efficiency for III-V multi-junction solar cells" by Dr. Shoou-Jinn Chang, Chair Professor of Institute of Microelectronics and Department of Electrical Engineering, National Cheng Kung University, Taiwan.

There were about 220 attendees at the mini-colloquium, including professors, IEEE members, students and local professionals in Taiwan.

~ Ming Liu, Editor

IEEE EDS Mini-Colloquium Organized by the ED Delhi Chapter

By R. S. Gupta and Sneha Kabra

The Department of Electronics, University of Jammu organized a one-day Mini-Colloquium National Seminar on "Advances in Electronic Devices and Circuits" in collaboration with the ED Delhi Chapter and IETE Jammu Centre on April 26, 2017. Three IEEE EDS Distinguished Lecturers delivered invited talks: Professor Subir Kumar Sarkar, Department of Electronics and Telecommunication Engineering, Jadavpur University, Calcutta, Professor Ajit Kumar Panda, National Institute of Science and Technology, Berhampur, Odisha and Dr. Manoj Saxena, Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi. Main focus areas of the seminar were Semiconductor Devices, VLSI Design and Technology, Nanoelectronics, Optoelectronics Devices and Sensors, MEMS and Digital Signal Processing, Low Voltage Analog and Digital Circuits, Embedded Systems, and Applied Physics and Material Science. This event was attended by approximately 150 participants from various academic institutions, including faculty members, research scholars and students of the host department and co-sponsored by J and K Bank, Ltd. and J and K State Science Technology and Innovation Council.

Dr. Subir Kumar, Dr. Rakesh Vaid, Dr. Ajit K Panda and Dr. Manoj Saxena at the University of Jammu

IEEE EDS Mini-Colloquium Organized by the ED Nepal Chapter

By Bhadra Prasad Pokharel

The chapter organized a Mini-Colloquium on May 23, 2017, at Materials Science and Engineering, Pulchowk Campus. Dr. Samar Saha, EDS President, delivered his inaugural talk on *"Modeling process variability for variability-aware integrated circuit design"* followed by Professor Chandan Sarkar's talk on *"Advanced heterostructure based nanoscale MOSFETs."* In the post lunch session, Dr. Xing Zhou, School of Electrical

Attendees of the ED Nepal Mini-Colloquium

and Electronic Engineering, Nanyang Technological University, Republic of Singapore discussed *"Future III-V/CMOS co-integrated technology and hybrid circuit design."* The program was supported by Pulchowk Campus, Institute of Engineering, the Nepal Physical Society, Golden Gate International College, Advanced College of Engineering and Management and Sagarmatha Engineering College. Fifty-five students and faculty members attended the program, including members of the Nepal Physical Society.

~ Manoj Saxena, Editor

Dear EDS Chapters:

When planning your upcoming chapter meetings, workshops, etc., please remember to visit the EDS website for a recent list of EDS Distinguished Lecturers and lecture topics.

✓ **Checklist**

- Chapter contacts EDS DL to check availability, confirms date/location of lecture, discusses DL funding needs and determines chapter funding
- EDS DL completes EDS DL Activity Log and Funding Request Form
- If applicable, obtain EDS funding approval
- Chapter publicizes lecture via web, email, etc. Obtain a chapter member list via SAMIEEE (http://www.ieee.org/about/volunteers/samieee/index)
- If applicable, DL submits an IEEE expense report to Laura Riello, to receive reimbursement
- Chapter Chair/DL Coordinator submits an EDS DL/MQ Feedback Form

If you have any questions and/or need more information, please do not hesitate to contact Laura Riello, EDS Executive Office.

Thank you for your continued support of the Society.

USA, Canada & Latin America (Regions 1-6, 7 & 9)

ED Mid-Hudson Valley Chapter

—by Mukta Ghate Farooq

On March 22, 2017, we organized a Distinguished Lecture given by Prof. Subramanian Iyer of UCLA on *"Forget about SoCs – Lets talk about SoWs."* His talk was well attended locally by about 50 people at the GlobalFoundries site in Fishkill, New York, and remotely by 20 people at Yorktown, New York and Burlington, Vermont. There were about 20 IEEE EDS members among the audience.

The abstract of the talk was as follows: "Silicon features have scaled by over 1500X for over five decades, which has spawned a vibrant system-on-chip (SoC) approach, where progressively more function has been integrated on a single die. However, as SoC's have become bigger and more complex, the Non-Recurring Engineering Charge and time to market have both ballooned out of control leading to ever increasing market consolidation. At UCLA, we are trying to address this problem through novel methods of system Integration. We show that with the apparent slowing down of semiconductor scaling and the advent of the Internet of Things, there is a focus on heterogeneous integration and system-level scaling. Packaging is undergoing a transformation that focuses on overall system performance through integration rather than on packaging individual components. We propose ways in which this transformation can evolve to provide a significant value at the system level while providing a significantly lower barrier to entry compared with a chip-based SoC approach that is currently used. More importantly, it will allow us to re-architect systems in a very significant way. This transformation is already under way with 3-D stacking of dies and will evolve to make heterogeneous integration the backbone of a new SoC methodology, extending so we can integrate entire Systems on Wafers (SoWs). We will describe the technology we use and the results to-date. This has implications in redefining the memory hierarchy in conventional systems and in neuromorphic systems. Additionally, we will look at anew at conventional devices and explore new ways to use them in in memories, neuromorphic computing, fault-tolerance and repair applications in the CHIPS context. We extend these concepts to flexible and biocompatible electronics."

On July 26, 2017, we arranged a Distinguished Lecture on Physics of III-N-based Field Effect Transistors by Prof. Michael Shur of Rensselaer Polytechnic Institute, at the Globalfoundries site in Fishkill, New York. A total of 15 people attended, both on site and remotely; of these about 8 people were IEEE EDS members.

The abstract of Prof Shur's talk was as follows: "Wurtzite (hexagonal) symmetry makes the device physics of GaN/AlN/InN heterostructure field effect transistors (HFETs) to be quite different from that of more conventional GaAs/InAs/InP and Si FETs. Spontaneous and piezoelectric polarization at AlGaN/GaN and AlGaInN/InGaN interfaces leads to the formation of two-dimensional (2D) electron gas with concentrations 10 to 20 times higher than that for more conventional FETs and with enhanced electron mobilities but a reduced peak velocity. Quantum well designs (incorporating AlN spacers an InGaN quantum well between the wide band gap AlGaN barrier layer and GaN buffer) have been used to control the electron transfer from the 2D channel into adjacent layers. High electric fields at the gate edges leads to an additional strain and hot electron effects causing the current collapse and gate lag. Large electron densities in the HFET channels minimize 1/f noise making it to be smaller than even in highly doped GaN films. This device physics necessitates new approaches to the device design. Inverted HFET devices are expected to have a reduced access resistance, a larger current carrying capability, lower gate leakage and a better thermal control. Insulated gate heterostructure field effect transistors demonstrated superior performance and reliability. Field plates, recessed and double recessed gates, drain field controlled electrodes, and Low Conducting Layers (LCLs) control current collapse and improve device reliability. Power and RF switching applications of III-N based transistors have emerged to take advantage of superior current carrying capabilities, low access resistance, and high breakdown voltage."

ED/AP/MTT Cleveland

—by Maximilian C. Scardelletti

The IEEE Electron Devices Society Cleveland Chapter and the IEEE Cleveland Section hosted Dr. Renuka "Ray" P. Jindal where he presented his lecture entitled "*From millibits to Terabits per second and Beyond -Over 60 years of Innovation"* at NASA Glenn Research Center in Cleveland, Ohio and the Play Arcade and Kitchen entertainment center in Mayfield, Ohio. Both lectures were held on May 16, 2017, from 10:30 to 11:30 AM and 5:00 to 8:00 PM at NASA and Play Arcade and Kitchen, respectively. The two events attracted over 70 attendees in total and 45 were IEEE student and higher grade members.

Maximilian C. Scardelletti, Chapter Chair (left), Renuka Jindal (center), and Drew Hayes (right), Cleveland Section Chair

Dr. Jindal's lecture described the advancement of telecommunications from the development of the p-n junction in 1940 by Ohl and the junction transistor in 1948 by Shockley to advancements of modern day communications. He also discussed his experiences working at Bell Laboratories and the advancements in communications he and his colleagues contributed to. The benefits of IEEE membership was also discussed with the students and Young Professionals in attendance, who also provided feedback regarding opportunities to improve IEEE membership for their demographics. The two lectures received very high reviews from the attendees and were very interactive with Dr. Jindal answering questions throughout both of the presentations. Dr. Jindal is currently a Professor in the Electrical and Computer Engineering Department at the University of Louisiana at Lafayette, Lafayette , Louisiana and he the is an IEEE Division I Delegate-Elect/Director-Elect, 2017, and IEEE Division Delegate/Director, 2018–2019.

~ Mukta G. Farooq, Editor

University of Sao Paulo, Brazil

—by Joao Antonio Martino

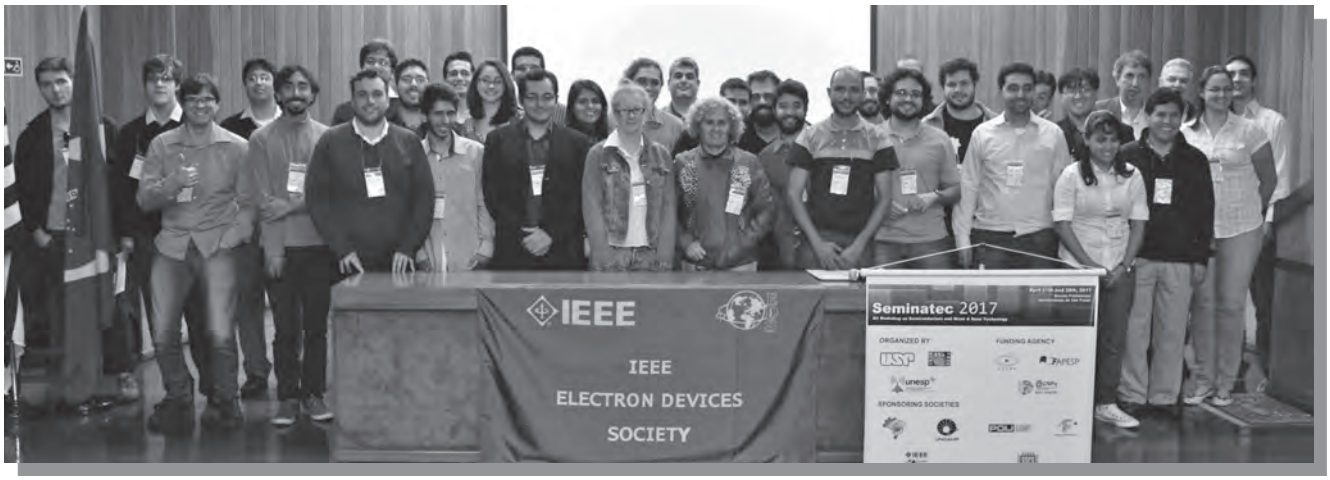
The ED South Brazil Chapter organized the XII Workshop on Semiconductors and Micro & Nano Technology (SEMINATEC 2017), held on April 27–28, 2017, at University of Sao Paulo, Brazil. It was co-organized by Integrated Systems Laboratory at the University of São Paulo (USP), Sao Paulo State University (UNESP – campus of Sao Joao da Boa Vista, Brazil), EDS Student Chapter of Campinas State University (UNICAMP), EDS Student Chapter of FEI, IEEE Solid-State Circuits Society, and the Brazilian Microelectronic Society.

The purpose of SEMINATEC is to promote interaction among industry, academy, research and development centers, government and students, all looking for real opportunities towards improving semiconductor and micro & nanotechnologies, research, and education. More than a hundred and twenty participants attended SEMINATEC 2017 from academia, research institutes, and industry. Such relatively high attendance reflects the enormous success of its organization, and indicates the substantial and growing interest over the years. This year, SEMINATEC's two days intense program was centered on six overview lectures listed below, four of which were EDS Distinguished Lecturers and one SSCS Distinguished Lecturer:

1) *"Material and Device Challenges for the End of the Roadmap CMOS Technologies,"* by Prof. Cor Claeys, K.U. Leuven and Imec, Belgium (DL invited by EDS South Brazil Chapter/USP).
2) *"Do much with very little: micropower management for energy harvesting applications,"* by Prof. Enrico Sangiorgi, Bologna University, Italy (DL invited by EDS South Brazil Chapter/USP).
3) *"Low frequency noise as a diagnostic tool in advanced MOSFET t*echnologies," by Prof. Bogdan Cretu, CAEN University, France (invited by EDS South Brazil Chapter/USP).
4) *"NanoMEMS: Enabling the Internet of Things,"* by Prof. Hector J. De Los Santos, NanoMENS Research, CA, USA (DL invited by EDS Student Branch of Campinas/UNICAMP).
5) *"FOSS TCAD/EDA tools for semiconductor device modeling,"* by Dr. Wladyslaw Grabinski, MOSAK Association EU (DL invited by EDS Student Branch of FEI).
6) *"Ultra low-power analog front-end design,"* by Prof. Pieter Harpe, Eindhoven University of Technology, Netherlands (DL invited by SSCS/USP).

In addition to the scientific lectures, five semiconductor companies were invited to give half-hour presentations describing their activities and areas of demands for research and human resources to academia and industry in the region. The microelectronic companies were the CEITEC silicon plant (a Federal research center), Smart Modular Technologies, Agilent Technologies, UNITEC Silicon Plant, and Brazil Components.

SEMINATEC 2017 Lecturers and organizing committee members (from left to right, sitting) Wilhelmus Noije, Paula Agopian (Program Chair), Enrico Sangiorgi, Cor Claeys, Hector De Los Santos, standing: Pieter Harpe, Marcelo Pavanello, Newton Frateschi, Alexandre Diniz, Wladyslaw Grabinski, Bogdan Cretu, Joao Martino (General Chair)



SEMINATEC 2017–Flash Presentations of Posters/Authors at University of Sao Paulo, Brazil

There was also a Poster Session where 51 selected technical papers were presented and discussed. SEMINATEC 2017 included a cocktail reception offered to all the participants.

More details about the program and the lecturers are available at http://www.psi.poli.usp.br/seminatec2017.

DL Presentation of Prof. Cor Claeys at University of Sao Paulo, Brazil, for undergraduate students

ED South Brazil Chapter

—by Paula Ghedini Der Agopian

The ED South Brazil chapter organized a series of Distinguished Lectures by Prof. Cor Claeys during the period of April/May 2017, at Polytechnic School at University of Sao Paulo, Brazil.

Prof. Cor Claeys performed the following presentations at University of Sao Paulo:

Title 1: *"Noise as a tool for MOSFET Electrical Characterization (part 1 – Basic)"*

Date: 17/04/2017, Number of attendees: 30 Master and Ph.D students.

Title 2: *"Microelectronics Impacting Society and Everyday Life"*

Date: 20/04/2017, Number of attendees: 30 4th year undergraduate students of Electronic and Systems;

Date: 02/05/2017, Number of attendees: 120 3rd year undergraduate students of Electrical Engineering.

Title 3: *"Noise as a tool for MOSFET Electrical Characterization (part II-Advanced)"*

Date: 24/04/2017, Number of attendees: 30 Master and Ph.D students.

Title 4: "Micro/Nanoelectronics devices: Present and Future in terms of research topics"

Date: 05/05/2017, Number of attendees: 20 researcher of SOI CMOS group of University of Sao Paulo, Brazil.

We had IEEE EDS members, undergraduate and graduate students

DL Presentation of Prof. Cor Claeys at University of Sao Paulo, Brazil, for graduate students

from University of Sao Paulo and several universities in the region. It was very important for the region to have the presence of Prof. Cor Claeys for one month, giving lectures and participating in many technical meetings with Prof. Joao Martino's research group and others.

Some of the participants gathered during the Conference Banquet on ICCDCS 2017

2017 ICCDCS

—by Roberto Murphy and Jacobus Swart

From June 5–7, 2017, the Tenth edition of ICCDCS (2017 International Caribbean Conference on Devices, Circuits and Systems) was held on the island of Cozumel, Mexico. This edition was dedicated as a homage to Dr. Eugeni Garcia, a teacher and researcher at the University of the Balearic Islands in Majorca, Spain, who regretfully passed away this last February. Dr. Garcia was one of the most fervent promoters of ICCDCS and academic collaboration between Europe and the Americas, as well as an active EDS participant throughout his professional life.

ICCDCS 2017 was organized by the INAOE, in Puebla, Mexico, with the technical and financial sponsorship of EDS, the CONACYT, and the Iberoamerican Science and Technology Education Consortium.

During the conference, 27 papers covering a gamut of modern electronics were presented, as well as six key-note lectures by world renowned scientists: Jürgen Becker, from the Karlsruhe Institute of Technology in Germany, whose talk was focused on Adaptive Heterogenous Multi-Core Technologies. Dr. Malgorzata Chrzanowska-Jeske, from Portland State University spoke of 3D integration. Dr. Filipe Vinci, based on the Centrale Supelec in France gave a talk on modeling and verification of heterogeneous systems. Dr. Jacobus Swart, who serves as an elected member in the EDS Board of Governors, lectured on Innovation by ASIC design and emerging sub-stream markets. While Dr. Adelmo Ortiz-Conde, from the Simon Bolivar University in Caracas, and founder of ICCDCS, presented a talk on the various techniques available to extract parameters from MOSFET measurements to model series resistance and mobility using only one device. The highlight of the keynote speeches was given by Dr. Benjamin Iñiguez, from the Universitat Rovira I Virgili, Tarragona, Spain, who talked about the "Life and Times of Eugeni Garcia", as he was one of his first doctoral students, and got to know him very well.

Fernando Guarin and Jacobus Swart presented the EDS Chapter of the Year award to the ED Spain Chapter for 2016. They noted that getting this award was largely due to Eugeni's work in the region, and motivated Dr. Benjamin Iñiguez to continue on the same path.

Presentation of the Chapter of the Year Award. (from left to right) Fernando Guarin , Benjamín Íñiguez, Jacobus Swart

ED Brazilian Chapter Meeting

—by Joao Antonio Martino

The ED South Brazil Chapter and the EDS Subcommittee for Regions/Chapters – Region 9, organized the ED Brazilian chapter meeting on June 5, 2017, at the University of Sao Paulo, Brazil.

It had the participation of the following ED chapters: (i.) ED student chapter of the Universidade Federal do Vale do São Francisco, BH, Brazil, (ii.) ED student chapter of the Universidade Federal da Bahia, Salvador, BH,

Chapter Chairs on the left and the visit of the researches laboratories at University of Sao Paulo on the right

Brazil, (iii.) ED student chapter of the Universidade Estadual de Campinas (UNICAMP), Campinas, SP, Brazil, (iv.) ED Student chapter of Centro Universitario da FEI, Sao Bernardo do Campo, SP, Brazil, (v.) and ED South Brazil Chapter of the University of Sao Paulo (USP), Sao Paulo, SP, Brazil.

After the activities reports presented by each chapter, they visited the Electron Devices Laboratories of the University of São Paulo and finished by discussing how to improve the ED activities for Region 9.

ED/CAS/PEL Venezuela Chapter

—by A. Ortiz-Conde

A technical lecture was held on Tuesday July 11, 2017, at Simón Bolívar University, Caracas, Venezula. The invited lecturer was Ramón Salazar, who talked on the topic of *"Modeling Tunnel Effect, from Feynman to WKB to Fowler-Nordheim."* Ramón obtained a PhD at Purdue University, USA, under the guidance of Prof. Joerg Appenzeller and he is presently working at GlobalFoundries in Malta, New York, USA.

This interesting lecture unambiguously clarified what is the tunneling effective mass that must be used in the well-known WKB and Fowler-Nordheim equations as carriers tunnel between conduction and valence bands (band-to-band tunneling). This is achieved by using Feynman's general formulation of quantum mechanics containing "Path Integrals" and establishing the correct approximations (e.g., imaginary dispersion branches with elliptic curvature) that lead to an accurate mathematical description of the tunneling phenomenon.

There was a very lively involvement of the audience in discussions, and the many interesting questions and answers motivated additional informal meetings which took place after the conclusion of the official seminar.

For additional information contact Professor Adelmo Ortiz-Conde at ortizc@ieee.org.

~Joao Antonio Martino, Editor

Europe, Middle East & Africa (Region 8)

ED Poland Chapter

—by Krzysztof Gorecki

The ED Poland Chapter held a meeting during the MIXDES 2017 Conference, which was held June 23, 2017, in Bydgoszca. The meeting was opened by the Section President, Professor Andrzej Rybarczyk, followed by an invited lecture entitled, DSc. Paweł Śniatała from Poznań University of Technology presented the invited lecture entitled *"Microelectronics in healthcare applications," by DSc. Pawel Sniatala, Poznan University of Technology.*

Later it was proposed to organize a special session devoted to applications of electronics in medicine as a part of the 2018 MIXDES Conference in Gdynia. Additionally, Professors Witold Pleskacz and Andrzej Napieralski shared information about other conferences which will be organized in 2018 by the ED Poland Chapter.

~ Mariusz Orlikowski, Editor

ED Scotland

—by Anthony Walton

In July, the Scottish Chapter of the IEEE Electron Devices Society held its third annual *Evening's Exploration of Past, Present and Future Electronics*. The event marked the passing of the Chapter Chair role from Prof. Anthony Walton of the University of Edinburgh to Prof. Marc Desmulliez, Head of Sensors, Signals and Systems at Heriot-Watt University. The event also celebrated the recent elevation of John Thompson, Professor of Signal Processing and Communications at the University of Edinburgh, to IEEE Fellow. Prof. Thompson gave a fascinating talk entitled "*Adventures in Wireless Communications towards 5G,*" to an audience of nearly 100 engineers, academics and members of the public. John specialises in cooperative communications systems, energy efficient wireless communications and antenna array processing. He entertained the audience with a talk that looked at the major advances in wireless communications over the last twenty years, advancing through the generations and finishing with his perspective of what can be expected from fifth generation (5G) wireless communications.

The talks were followed by a drinks reception in the University of Edinburgh's James Clerk Maxwell

Ramón Salazar during his presentation and with a part of the audience

The Evening's Speaker, Professor John Thompson (left), with outgoing ED Scotland Chair, Professor Anthony Walton and incoming Chair, Professor Marc Desmulliez (right)

Building at which guests were able to enjoy an exhibition of tabletop displays. Professor Tom Stevenson, Chair of the Museum of Communication in Burntisland (www.mocft.co.uk) brought a collection of telephone and radio systems for the audience to interact with. There were also demonstrations from Christian Nunez-Alvarez of Keysight Technologies and a number of John's current cohort of researchers. The organizers would like to thank all those that attended for helping to make it a fun, informative and memorable evening.

~ Jonathan Terry, Editor

Joint Activities of the IEEE Ukraine Section Chapters

IEEE 37th International Conference on Electronics and Nanotechnology (ELNANO-2017)

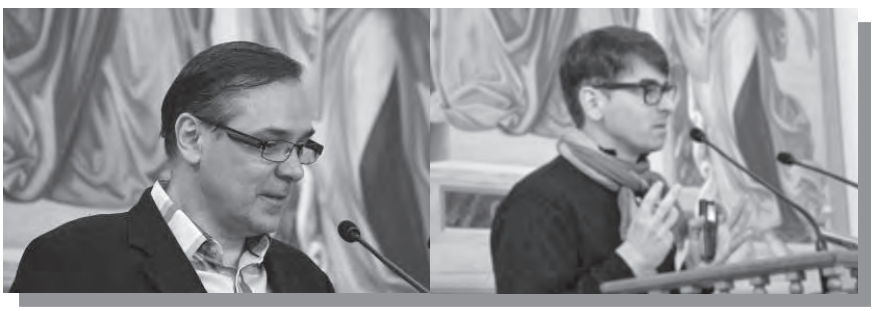
—by Kateryna Ivanko, Nikolay Cherpak, and Kateryna Arkhypova

The IEEE 37th International Scientific Conference on Electronics and Nanotechnology (ELNANO-2017), was held April 18–20, 2017, at the National Technical University of Ukraine's Igor Sikorsky Kyiv Polytechnic Institute. It was co-sponsored by the IEEE Ukraine Section and five of the Section's Chapters. The IEEE Ukraine Section (Kyiv) ED/MTT/CPMT/SSC/COM Chapter and the IEEE Ukraine Section (East) AP/MTT/ED/AES/GRS/NPS Chapter were financial and technical sponsors, respectively.

The conference program consisted of the Plenary sessions and three Section sessions: *"Micro- and nanoelectronics," "Biomedical Electronics and Signal Processing,"* and *"Electronic systems;"* as well as a Poster session and two half-day Seminars: *"Implementation of Embedded Linux in Systems-On-Chip With Nios Ii Processor,"* held by Ievgen Korotkyi, Associate Professor of Department for Design of Electronic Digital Equipment, Igor Sikorsky Kyiv Polytechnic Institute, *and "Quartus II Incremental Compilation and Logiclock Technology,"* by O. Antonyuk, Senior Lecturer, in the same department. A total of 128 works were submitted for presentation at the conference and 111 submissions were accepted. There were 74 oral talks and 37 poster presentations. The full list of the authors contained 370 researchers from 19 countries, namely from Armenia (19), Australia (1), Belgium (1), Canada (2), Czech Republic (1), France (4), Italy (7), Korea (2), Libya (1), Lithuania (1), Mexico (3), Netherlands (3), Norway (2), Poland (19), Russia (23), Spain (1), Turkey (5), USA (11), Ukraine (267). Finally, 137 researchers attended the conference. The working language of the conference was English.

During the conference many interesting reports were presented on the development of modern nanotechnology, micro- and nano-electronic components, and methods for electronic circuit and system design.

The IEEE ELNANO-2017 opening speeches by Prof. Michael Zgurovsky, Rector of Igor Sikorsky Kyiv Polytechnic Institute (left) and Prof. Yuriy Yakymenko, First Vice Rector of Igor Sikorsky Kyiv Polytechnic Institute and General Chairperson of ELNANO-2017 (right)



Plenary talks by Prof. Roderick Melnik, Wilfrid Laurier University, Canada (left) and Dr. Guillaume Brotons, University Le Man, France (right)

Also, the latest developments were reported on processing of signals and images, electronic systems, prospects for development of biomedical devices and systems, and on the use of nanotechnology in biomedical electronics. There were fruitful scientific debates to discuss the possibilities of international cooperation and implementation of joint research projects, involving a wide range of national and international scientific organizations.

The Conference Proceedings are published in English, and can be found in the IEEE *Xplore* Digital Library and indexed by Scopus and Web of Science. Visit the conference website for more information, *http://elnano.kpi.ua*.

The first IEEE Milestone ceremony in Ukraine was held during IEEE UKRCON-2017

IEEE First Ukraine Conference on Electrical and Computer Engineering (UKRCON-2017)

—by Nikolay Cherpak, Kateryna Ivanko, and Mykhaylo Andriychuk

The IEEE Ukraine Conference on Electrical and Computer Engineering (UKRCON-2017) was founded by the IEEE Ukraine Section and was held May 29–June 2, 2017. The IEEE UKRCON-2017 was co-sponsored by IEEE Region 8 and almost all IEEE Ukraine Section Chapters. The IEEE Ukraine Section (East) AP/MTT/ED/AES/GRS/NPS Chapter, the IEEE Ukraine Section (Kyiv) ED/MTT/CPMT/SSC/COM Societies and IEEE Ukraine Section (West) MTT/ED/AP/CPMT/SSC Chapter were the technical sponsors and financial supporters.

The IEEE UKRCON-2017 opening speeches by Chairperson of the IEEE Ukraine Section, Prof. Felix Yanovsky (left,) and one of the distinguished guests Prof. Roberto Sorrentino IEEE Fellow, EuMA co-founder and ex-President, 1998–2009 (right)

The IEEE UKRCON-2017 Opening Ceremony, May 29, 2017, Kyiv, Ukraine

The objective for this conference was to establish the IEEE Section flagship conference in Ukraine as a high quality scientific platform for discussion and cooperation. The topic of the event was the Celebration of the 25th Anniversary of the IEEE Ukraine Section. In November 1991, the IEEE Ukraine Section was founded at the Igor Sikorsky Kyiv Polytechnic Institute in cooperation with the Ministry of Education of Ukraine and with Canadian scientists. Therefore, the Igor Sikorsky Kyiv Polytechnic Institute was chosen as the first symbolic venue for the IEEE Ukraine Section flagship conference.

Over 250 persons from over 80 organizations and 19 countries gave their time and resources to attend and to contribute. Among them, distinguished guests: Prof. Vincenzo Piuri, IEEE Vice-President for Technical Activity (Milan University, Italy); Prof. Roberto Sorrentino, IEEE Fellow, European Microwave Association (EuMA) co-founder and past President (University of Perugia, Perugia, Italy), Mr. Costas Stasopoulos, Past Director of the IEEE Region 8 (Nicosia, Cyprus), and Dr. Gerard Rankin (Adelaide University, Australia).

In addition, the first IEEE Milestone ceremony in Ukraine was organized at *UKRCON*. It was a huge historical event for the Ukrainian scientific community. The IEEE Milestone title *is "Zenit three-coordinate L-band pulsed radar, 1938."* It is dedicated to the Zenit parabolic reflector L-band pulsed radar developed in 1938, in Kharkiv, which was able for the first time to measure three coordinates of a target.

IEEE Ukraine Section (East) AP/MTT/ED/AES/GRS/NPS Chapter

—by Nikolay Cherpak and Kateryna Arkhypova

Several times a year, our Chapter holds technical meetings with the themed presentations at the Usikov Institute for Radiophysics and Electronics NASU in Kharkiv. These meetings cover multiple topics concerning all aspects of engineering, theoretical and experimental physics, electron devices, semiconductors, etc. This year, we have already held nine such meetings.

~ Daniel Tomaszewski, Editor

Mini-Colloquium on Semiconductor Device Technologies and Compact Modeling

On Tuesday, February 7, 2017, the Electron Devices Society organized a mini-colloquium linked to the 11th Spanish Conference on Electron Devices (CDE), held in Barcelona, February 8–10, 2017. The Chairs of the mini-colloquium were Prof. Lluís F. Marsal (ED Spain Chapter Chair) and Prof. Benjamin Iñiguez, both from Universitat Rovira i Virgili (URV), Tarragona, Spain. Four invited speakers, all of them EDS Distinguished Lecturers, conducted talks ranging from semiconductor device technologies to compact modeling.

Prof. J.-H. He, from the King Abdullah University of Science and Technology, Saudi Arabia, gave a presentation entitled *"Flexible, Foldable and Multi-Functional Paper-Based Electronics."* Prof. E. Miranda, from the Autonomous University of Barcelona (UAB), targeted the compact modeling of hysteresis effects in RRAM devices. Prof. B. Iñiguez (URV, Spain) addressed the compact modeling and parameter extraction of Amorphous Oxide TFTs. Finally, Prof. L. F. Marsal (URV, Spain) gave a talk entitled *"Fabrication of nanostructured polymers for organic solar cells."*

Lluis F. Marsal
Universitat Rovira i Virgili
Tarragona, Spain

~ Jan Vobecky, Editor

Asia & Pacific (Region 10)

ED Kansai

—by Michinori Nishihara

The ED Kansai Chapter held the 15th International Meeting for Future of Electron Devices, Kansai (2017IMFEDK) at Ryukoku University Kyoto Hall, Kyoto, Japan, June 29–30, 2017, with the theme of "Electron Devices and Intellectualization of Everything."

The meeting attracted 98 attendees and was preceded by a tutorial seminar with two Distinguished Lecturers: 1) *"Development of Spintronics and Device Application,"* by Prof. Yasuo Ando of Tohoku University, and 2) *"H/W Technology for Cognitive Computing,"* by Dr. Koji Hosokawa of IBM Japan. The formal program began after the tutorial session with opening remarks by the general chair, Prof. Yasuhisa Omura. The two-day program featured a keynote titled *"Neuromorphic System for Next Generation AI,"* by Prof. Takashi Kohno of the

2017 IMFEDK Awards Winners

IMFEDK Poster Session

University of Tokyo. There were also five invited papers: 1) *"Silicon Thermoelectric Generator Fabricated By CMOS Compatible Process,"* by Prof. Takanobu Watanabe of Waseda University; 2) *"Recent Topics of Vertical GaN Power Devices,"* by Dr. Tohru Oka of Toyoda Gosei; 3) *"Characterization of lightly-doped n- and p-type homoepitaxial GaN on free-standing substrates,"* by Prof. Masahiro Horita of Kyoto University; 4) *"MEMS Mirrors for automotive applications,"* by Prof. Toshiyuki Tsuchiya of Kyoto University; and 5) *"Wearable, Healthcare Sensor Sheets,"* by Prof. Kuniharu Takei of Osaka Prefecture University.

In addition, there were 12 papers in three regular technical sessions and a poster session of 24 posters with topics encompassing Silicon, Compound, and Emerging Technologies. There were many students in discussions in front of their posters during the poster session.

At the end of the meeting, the following awards were presented:

- IEEE EDS Kansai Chapter IMFEDK Best Paper Award to Dr. Hideki Iwamoto of Murata Manufacturing Company, Ltd. and Dr. Katsuyuki Sakurano of Ricoh Company, Ltd.
- IEEE EDS Kansai Chapter IMFEDK Student Paper Award to following five persons: Mitsuhiro Urano (National Institute of Technology, Naga College), Wataru Gamachi (University of Fukui), Daisuke Tahara (Kyoto Institute of Technology), Shotaro Shinya (Osaka Institute of Technology).

All participants warmly congratulated the award winners. IMFEDK will continue to encourage and contribute to our student members in the Kansai area by providing opportunities to present their ideas in English, hence extend their technical network to other countries.

~ Kuniyuki Kakushima, Editor

ED Dalian Chapter

—by Zhengxing Huang

The ED Dalian Chapter organized a seminar about new approaches to high-frequency acoustic wave devices on June 7, 2017. Prof. Zhiming Chen from Toyama Prefectural University of Japan was the keynote speaker. About thirty attendees, including most IEEE members in our chapter, took part in this seminar.

Prof. Chen introduced the following content: the development and working frequency of the surface acoustic wave (SAW) from a material perspective, multi-layer SAW based on substrates with high acoustic speed, the Flexural Plate Wave (FPW) and high-order FPW in thin slides, etc.

The seminar was supported by the international cooperation project of the National Natural Science Foundation of China.

ED/SSC Nanjing Chapter

—by Weifeng Sun

The ED/SSC Nanjing Chapter held two special Distinguished Lectures (DLs) on April 21st, hosted by Prof. Mingxiang Wang of Soochow University. The two experts were both from the National Chiao Tung University, Taiwan. The first lecture, given by Prof. Pei-wen Li, entitled *"Germanium enablers for electronics and photonics convergence in CMOS Si platform"* gave a background review on the important milestones of Ge in semiconductor devices. Prof. Li then presented recent advances in Ge quantum dot growth and devices supporting the Si nanoelectronics and photonics. Her team had successfully exploited multi-dimensional spaces of temperature, concentrations of the three interstitial species, Si, Ge and O, geometries and compositions of the starting SiGe nano-pillar substrates, sources of Si interstitials to create new classes of exciting optical and electronic de-

(left) P-W Li (speaker); (middle) (from left) the seminar chair, Mingxiang Wang (4th), H-C Lin (5th, speaker), P-W Li (6th, speaker) speakers and the audience; (right) speakers with university faculty

vices, such as single-electron tunneling devices, nonvolatile memories, wavelength-tunable photodetectors, and "Instant" (Single Step Fabrication) MOSFETs.

The second DL, by Prof. H. -C Lin, *"BEOL Metal-Oxide Transistor Technology for Newly Emerging Applications"* introduced background on the development of oxide-semiconductor-based TFT technology for new applications of BEOL active devices embedded in IC chips, followed by information on a new film-profile-engineering (FPE) concept that the team developed a few years back in fabricating the BEOL oxide-based devices. Several processes developed to demonstrate the FPE devices with sub-micron or nanometer-scaled channel lengths, were subsequently presented. He also shared experiences about the selection of deposition tools and the adjustment of deposition conditions with the attendees. The FPE approach has also been employed for studies of various device topics, including high-voltage transistors, inverters, and sub-50 nm transistors. In the end, this talk also addressed the issues and feasibility of the FPE approach for these applications.

This event had quite good attendance, with approximately 70 senior undergraduate and graduate students, 10 faculty members and postdoctoral researchers.

(left) Mandar Bhoir (speaker); (right) the speaker with ED NCTU student members

ED Taipei Chapter

—by Steve Chung

The ED Taipei Chapter together with the ED NCTU Student Chapter, held one invited talk in the second quarter of 2017. A DL on May 3rd, by Mandar Bhoir, a PhD scholar of IIT Gandhinagar, India, titled *"Investigation of Frequency Behavior and Modeling of Gate-Leakage in Advanced FDSOI CMOS Technology,"* presented two interesting topics relating to the FDSOI CMOS. The first on an anomalous behavior observed from a UTB SOI, mainly the gm increases with the increasing frequency, which comes from the coupling between the gate and the substrate underneath BOX. This is useful for a proper design of UTB SOI. The second topic introduced was a new gate current modeling, different from the popular BSIM4 and BSIM6, by incorporating a suitable trap-assisted tunneling model, which can accurately describe the gate current in a high-k metal, gate CMOS. Around 20 graduate students, most of them IEEE student members, attended.

The premier event on VLSI in the region, as well as a leading technology conference worldwide for over 30 years, the VLSI-TSA and VLSI-DAT was held April 24–27, 2017, (http://expo.itri.org.tw/2017vlsitsa). Both are technically co-sponsored by the IEEE Electron Devices Society and the IEEE Solid State Circuits Society. The conferences attracted over 850 worldwide attendees in the technical sessions and more than 300 in a series of short courses, in which around 65% were from the industry and 35% from academia. Next year the conference will be held again in Hsinchu, Taiwan. The paper submission deadline is October 31, 2017, and more information can be found on the conference website, http://expo.itri.org.tw/2018vlsitsa. For further information, please contact Miss Evelyn Chou at vlsitsa@itri.org.tw.

Another conference, the IEEE EDSSC (International Conference on Electron Devices and Solid-State Circuits), scheduled for October 18–20, 2017, at National Tsing Hua University, http://www2.ess.nthu.edu.tw/edssc2017/, will have EDS as a co-sponsor and key members of the local chapter involved. The paper submission deadline has passed, however, researchers are encouraged to attend the conference.

ED Tsinghua University Student Branch Chapter

—by Yancong Qiao

The ED Tsinghua University Student Branch Chapter held an EDS Distinguished Lecture on March 21, 2017. The speaker, Prof. Faxian Xiu, from the Department of Physics, Fudan University, China, gave a talk titled, *"Electronic and optoelectronic devices based on two-dimensional materials and Dirac materials."* He briefly introduced the work in material growth, device preparation and application by his group, including epitaxial growth of large-scale two-dimensional material, preparation of heterojunctions and photoelectric detection and imaging. In the case of Dirac materials and novel (spin) electronic devices, he highlighted the material properties and device applications of graphene-like quasi-two-dimensional Dirac materials, such as zirconium telluride and three-dimensional system of cadmium arsenide. This talk was attended by around 20 graduate students, professors, and postdoctoral researchers.

ED Guangzhou Chapter

—by Zhangang Zhang

The ED Guangzhou Chapter held an EDS Distinguished Lecture on May 4, 2017, at South China University of Technology. Professor Juin J. Liou was invited to present a lecture titled *"Outlook and Challenges of Electro-*

Juin J. Liou (middle, the first row) and members of the ED Guangzhou Chapter

Prof. Hiroshi Iwai (first row, second from right) and the audience

static Discharge (ESD) Protection of Modern and Future Integrated Circuits." Prof. Liou gave an overview on the ESD sources, models, protection schemes, and testing, followed by the challenges of designing and realizing ESD protection solutions for integrated circuits in Si CMOS, Si BiCMOS, GaAs, GaN, and emerging technologies. Challenges and difficulties associated with the ESD design and optimization for these technologies were finally addressed. Academics, engineers, and students from institutions of Southern China area attended this event and enjoyed the discussions with Professor Liou.

ED Beijing Chapter
—by Kangwei Zhang

On May 4, 2017, Professor Hiroshi Iwai visited the ED Beijing Chapter. His Distinguished Lecture entitled, *"Recent progress of semiconductor power devices,"* was hosted by Prof. Ming Liu, the Chapter Chair. More than 40 local professionals and graduate students attended the lecture.

Wide gap semiconductor such as SiC and GaN have been regarded as the next generation materials to replace Si power devices, because of their superior nature for high breakdown voltage and high mobility/frequency operation. On the other hand, Si power devices are expected to keep the major market share for next 20 years because of their superiority in production cost. Recently, there are significant progress in both wide bandgap and Si power device technologies. Prof. Iwai presented the recent progress of power device technologies for SiC, GaN and Si based on the materials published at IEDM 2016.

~ Ming Liu, Editor

ED NIST Student Chapter
—Ajit K Panda

On June 1, 2017, the ED NIST Student Chapter organized a technical lecture on *"Scientist and Engineers: Innovation and Technology"* by *Mr. Uttam Kumar Sahu,* currently working as a scientist-E, at Defense Research and Development Laboratory (DRDO) Hydradabad.

On June 5, 2017, the chapter organized a technical lecture on *"Product Development using Embedded Systems"* by Professor Aurobinda Routray, who is currently working as a professor at IIT Kharagpur. His focus was on young engineers with innovative ideas and system implementation using embedded programming, which provides a quick solution for different requirements.

The chapter organized a four week workshop on *"VLSI Design*

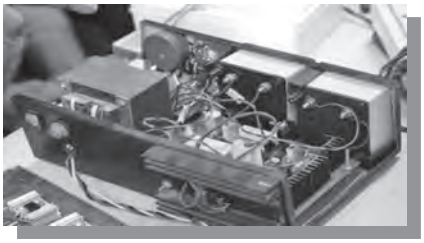
ED NIST Student Chapter workshop participants

and Automation Tools" from June 5–30, 2017, for students from Govt. Polytechnic Bhubaneswar and another workshop from June 24–July 20, 2017, for undergraduate students of NIST to enhance their VLSI Design skills.

ED Meghnad Saha Institute of Technology Student Branch Chapter

—by Manash Chanda and Swapnadip De

The ED MSIT Student Branch Chapter, MSIT Student Branch and ED Kolkata Chapter, in association with the Department of ECE, MSIT jointly organized the 2 day IEEE Workshop on Verilog A modeling and simulation with SPICE, at MSIT on April 17–18, 2017. Almost seventy-four students attended the event. Dr. Writam Banerjee, Institute. of Microelectronics, PR China, and Dr. Ambarnath Banerjee, MSIT, discussed various aspects of the Verilog Modelling and Simulation.



Prototype at the INNOVATION 2017

2nd MSIT Paper Contest at MSIT

The 2nd MSIT Student paper contest in the undergraduate category was organized on April 19–20, at MSIT, by the ED MSIT Student Branch Chapter, MSIT Student Branch and ED Kolkata Chapter, to motivate the students in research work. One hundred twenty-one students, including IEEE and non-IEEE student members, participated in the paper contest with almost forty-one papers presented in the contest. A two-day Innovation and prototype completion, INNOVATION 2017, was organized by the ED MSIT SBC, IEEE MSIT SB and IIEDS, MSIT on April 28–29, 2017. Twenty-five teams from different institutes participated to showcase their innovative prototypes. To spread the awareness of green technology, the Green Window Project competition was organized by the ED MSIT SBC, IEEE MSIT SB and Rotaract Club, MSIT on April 29, 2017. Fifteen school teams participated. Experts from industries attended the events to evaluate the performances of the INNOVATION 2017 and the Green Window project competitions.

ED Delhi Chapter

—R. S. Gupta and Sneha Kabra

The workshop on Industrial Automation and PLC was conducted by Sri Venkateswara College (University of Delhi) in association with the ED Delhi Chapter and Futuronix Automation Pvt. Ltd. on March 29, 2017. Basic information regarding the software "Twido Suite" and PLC, which is a virtual combination of relays, timers and counters was given. Ladder logic was explained and various logic gates were made with the help of ladder logic.

Educational visit to Semiconductor Laboratory, Chandigarh: April 12, 2017

The Department of Instrumentation, Shaheed Rajguru College, (University of Delhi) in collaboration with ED Delhi Chapter, organized an educational visit

Workshop on PLC and SCADA at Sri Venkateswara College (University of Delhi)

Prof. Fernando Guarin, EDS President Elect 2018 (center)

to Semiconductor Laboratory, Chandigarh, India on April 12, 2017. The ED Delhi Chapter provided technical support for this activity. Thirty-six students from B.Sc(H) Instrumentation IV sem and VI sem went for the visit along with 3 faculty members of the college. They learned about Design, Development, Fabrication, Assembly & Packaging, Testing and Quality Assurance of CMOS and MEMS Devices for various applications.

An IEEE EDS Distinguished Lecture on *"Reliability challenges for the qualification of Leading Edge CMOS Technologies,"* by Professor Fernando Guarín, Distinguished Member of Technical Staff, Global Foundries, East Fishkill, New York, and Adjunct Lecturer, SUNY, New Paltz, was organized at IIT, Delhi on May 19, 2017. The talk was jointly organized by IIT, Delhi and the ED Delhi Chapter. Through his talk, Prof. Guarin shared his vast experience in reliability qualification, which included both modeling and characterization, with undergraduate and postgraduate students and faculty members from various institutions.

AP/ED Bombay Chapter

—Anil Kottantharayil

The AP/ED Bombay Chapter organized three EDS Distinguished Lectures at IIT Bombay during the last quarter, with all of them receiving a tremendous response. The talks were attended by students, research staff and faculty of IIT Bombay, students and faculty members from educational institutions in and around Mumbai, and researchers and engineers from several companies in and around Mumbai.

The talks were delivered by EDS Distinguished Lecturers, Prof. Cary Yang, Fellow IEEE, Santa Clara University, USA; Dr. Bin Zhao, Fellow IEEE, Director of Engineering, ON Semiconductor, USA and Prof. Subramanian Iyer, Fellow IEEE, UCLA, USA, Director, Center for Heterogeneous Integration and Performance Scaling (CHIPS), who are eminent in their respective fields of research.

Prof. Cary Yang in his talk titled, *"All- Carbon Interconnects- From 1D to 3D,"* pointed out the critical challenges in chip manufacturing, among them, reliability and performance of on-chip interconnects and the measures to mitigate such challenges.

Dr. Bin Zhao in his talk titled, *"Power Management Solutions Enabled by Mixed-Signal Technologies and Intelligence,"* reviewed and discussed the challenges in power management and the innovative solutions enabled by mixed-signal design and technologies for the advantages in performance, power efficiency and cost.

Prof. Subramanian Iyer, in his talk titled, *"Packaging without the Package -A more Holistic Moore's Law,"* proposed ways in which the transformation in packaging can evolve to provide a significant value at the system level while providing a significantly lower barrier to entry when compared with a chip-based SoC approach that is currently used.

~ Manoj Saxena, Editor

Cary Yang (left of chapter banner), with the attendees of the EDS Distinguished Lecture

Attendees of EDS Distinguished Lecture at ED Poornima University Student Branch Chapter

EDS MEETINGS CALENDAR

The complete EDS Calendar can be found at our web site: http://eds.ieee.org. Please visit.

2017 12th European Microwave Integrated Circuits Conference (EuMIC)	08 Oct–10 Oct 2017	NÜRNBERG Convention Center (NCC) Messezentrum, NCC Ost Nuremberg, Germany
2017 IEEE International Integrated Reliability Workshop (IIRW)	08 Oct–12 Oct 2017	Stanford Sierra Conference Center 130 Fallen Leaf Road South Lake Tahoe, CA, USA
2017 International Semiconductor Conference (CAS)	11 Oct–14 Oct 2017	Rina Sinaia Hotel 8, Carol I Str. Sinaia, Romania
2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	16 Oct–19 Oct 2017	Hyatt Regency San Francisco Airport 1333 Bayshore Highway Burlingame, CA, USA
2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM	19 Oct–21 Oct 2017	Marriott Biscayne Bay 1633 N Bayshore Dr Miami, FL, USA
2017 Fifth Berkeley Symposium on Energy Efficient Electronic Systems & Steep Transistors Workshop (E3S)	19 Oct–20 Oct 2017	University of California, Berkeley Sutardja Dai Hall Banatao Auditorium Berkeley, CA, USA
2017 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)	22 Oct–25 Oct 2017	Miami Marriott Biscayne Bay 1633 N. Bayshore Drive Miami, FL, USA
2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)	30 Oct–01 Nov 2017	Hyatt Regency Tamaya Resort 1300 Tuyuna Trail Santa Ana Pueblo, NM, USA
2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	12 Nov–16 Nov 2017	Irvine Marriott 18000 Von Karman Ave. Irvine, CA, USA
2017 IEEE International Electron Devices Meeting (IEDM)	04 Dec–06 Dec 2017	Hilton San Francisco Union Square San Francisco, CA, USA

2017 IEEE 48th Semiconductor Interface Specialists Conference (SISC)	06 Dec–09 Dec 2017	Bahia Resort Hotel San Diego, CA, USA
2018 IEEE International Reliability Physics Symposium (IRPS)	11 Mar–15 Mar 2018	Hyatt Regency San Francisco Airport 1333 Bayshore Highway Burlingame, CA, USA
2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM)	13 Mar–16 Mar 2018	Kobe International Conference Center 6-9-1 Minatojima-nakamachi Chuo-ku Kobe, Japan
2018 19th International Symposium on Quality Electronic Design (ISQED)	13 Mar–14 Mar 2018	Santa Clara Convention Center 5001 Great America Pkwy Santa Clara, CA, USA
2018 Moscow Workshop on Electronic and Networking Technologies (MWENT)	14 Mar–16 Mar 2018	Ilya Ivanov 34 Tallinskaya Str. Moscow, Russia
2018 IEEE International Conference on Microelectronic Test Structures (ICMTS)	26 Mar–29 Mar 2018	TBD TX, USA
2018 IEEE International Vacuum Electronics Conference (IVEC)	24 Apr–26 Apr 2018	Monterey Marriott 350 Called Principal Monterey, CA, USA
2018 29th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	30 Apr–03 May 2018	Saratoga Springs City Center 522 Broadway Saratoga Springs, NY, USA
2018 7th International Symposium on Next Generation Electronics (ISNE)	07 May–09 May 2018	GIS TAIPEI TECH Convention Center (Building Everlight)2~3F., Ln. 193, Sec. 3, Zhongxiao E. Rd., Da'an Dist., Taipei City 106, Taiwan Taipei, Taiwan
2018 IEEE International Interconnect Technology Conference (IITC)	03 Jun–07 Jun 2018	Burlingame, CA, USA
2018 IEEE 45th Photovoltaic Specialists Conference (PVSC)	10 Jun–15 Jun 2018	Hilton Waikoloa Village 69-425 Waikoloa Beach Dr Waikoloa Village, HI, USA

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.